Low Power CNTFET 3-Transistor Approximate Full Adder for Real-Time Edge Image Processing

Dasamandam Venkata Supriya and Avireni Srinivasulu

***Abstract*—A low-power 3-transistor (3T) approximate full adder based on CNFET technology is proposed for edge image processing applications requiring low computational cost and compact area. The design emphasizes high power efficiency through an ultra-minimal transistor structure, which reduces circuit complexity while maintaining acceptable accuracy. Circuit-level performance is evaluated using a 32 nm CNFET model in the HSPICE simulator at a supply voltage of 0.9 V. The analysis considers key metrics such as power dissipation, propagation delay, power-delay product (PDP), and energy delay product (EDP). Results indicate power savings of about 35–40% and a delay reduction of approximately 55–60% compared to conventional approximate adders. Additionally, PDP improves by 75–80%, and EDP shows up to 90% enhancement. These improvements are mainly due to reduced transistor count and simplified routing paths. Although the design introduces approximation, the resulting accuracy remains within acceptable limits for error-tolerant image processing tasks. Overall, the proposed 3T CNFET full adder achieves an effective balance between power, delay, area, and computational accuracy.**

***Index Terms*—Approximate computing, Carbon nanotube field-effect transistor (CNFET), 3T full adder, Low- power VLSI design, Edge image processing.**

Original Research Paper
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I. Introduction

THIS rapid growth of real-time edge image processing applications, such as object detection, feature extraction, surveillance and autonomous systems, has intensified the demand for highly energy-efficient and area-constrained hardware architecture. Edge devices typically operate under strict power and resource limitations, making conventional accurate arithmetic circuits increasingly unsuitable due to their high-power consumption, large area overhead and complex routing structures. Consequently, there is a growing interest in alternative computing paradigms that can achieve substantial reductions in energy and hardware cost while maintaining acceptable computational performance. Approx-imate computing has emerged as a promising solution for error- tolerant applications, particularly in image processing, where perfect numerical accuracy is not always essential for perceptual quality. By deliberately relaxing accuracy constraints, approximate arithmetic circuits enable significant improvements in power efficiency, delay, and silicon area. Among arithmetic components, the full adder serves as a fundamental building block in digital signal processing units, image filters, and arithmetic logic units. Therefore, optimizing the full adder at the transistor level plays a critical role in enhancing the overall performance of image processing hardware. In parallel with approximate computing, emerging nano electronic technologies are being explored to overcome the limitations of conventional CMOS scaling [1]. CNFETs have gained considerable attention due to their superior electrical properties, such as near-ballistic transport, high carrier mobility, low leakage current and excellent scalability at deep nanometer nodes [2]. These features make CNFETs particularly well suited for low-voltage and low-power circuit designs intended for next-generation edge computing platforms. Recent studies have presented various approximate full adder designs using CMOS and CNFET technologies, aiming to improve energy efficiency by reducing transistor count and logic complexity [3]. However, many existing designs still suffer from relatively high propagation delay, increased routing complexity, or limited energy–accuracy optimization, which restricts their suitability for real-time edge image processing tasks. Hence, there remains a strong need for ultra-compact approximate adder architectures that can deliver superior power and delay performance without significantly compromising computational accuracy. Motivated by these challenges, this work presents a novel low-power 3T approximate full adder based on CNFET technology for real-time edge image processing applications. The new design employs an ultra-minimal transistor topology that significantly reduces circuit complexity, routing paths, and hardware overhead. Circuit-level simulations are performed using a 32 nm CNFET model in the HSPICE environment to evaluate key performance metrics, including power dissipation, propagation delay, Power Delay Product, and EDP at a supply voltage of 0.9 V. The results demonstrate that the new design achieves substantial improvements in power efficiency and energy-delay performance while maintaining an acceptable energy accuracy trade-off for approximate image processing tasks. Overall, the introduced CNFET-based 3T approximate full adder offers a compelling solution for low-power, area-efficient, and high-speed arithmetic units in real-time edge image processing systems.

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II. Related Work

Stringent restrictions have been mandated on power consumption, latency, and area based on the need to realize real-time image processing on edge devices such as mobile cameras, autonomous sensors, etc. Among these operators, adders are critical components that significantly influence overall edge computing efficiency. Approximate computing is receiving increased adoption to ease stringent accuracy constraints with respect to hardware efficiency, owing to the fact that image processing tasks are amply resilient to computation-precision-related issues.

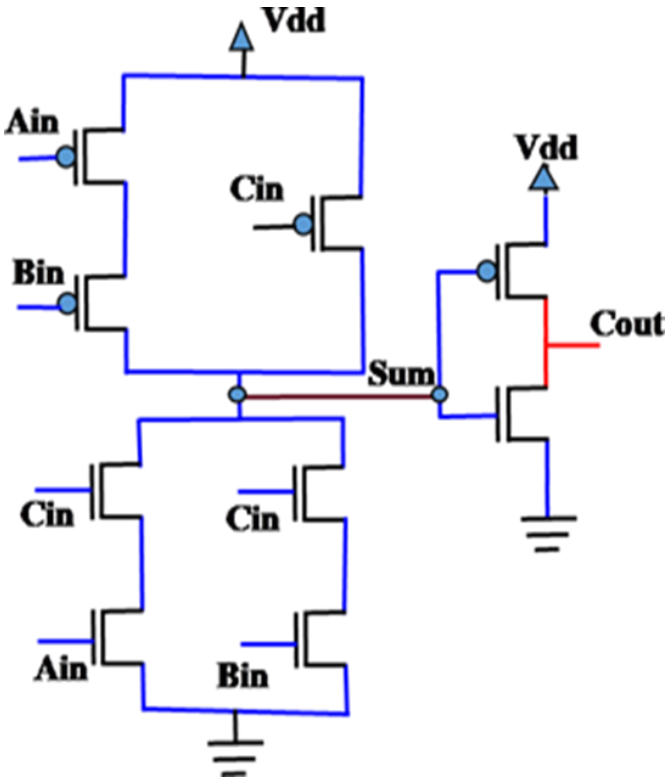
A. Approximate Full Adders in CMOS Technology

A substantial body of literature exists to describe approximation full adders (AFAs) designed using CMOS technology. The initial techniques had fewer transistors and switching activities due to simplification of Boolean equations of sum and carry outputs of adders. Compared to actual adders, several techniques like XOR/XNOR-based adders, transmission gate-based adders, and mirror adders reported similar improvements in power and area [4], [5]. Nevertheless, owing to short-channel effects and process corners and increased leakage currents due to increased submicron scaling techniques, approximation full adders based on CMOS techniques are difficult to scale deeper submicron geometries [6], [7]. Hence, it reflects their limitations in achieving low-power applications due to drastic degradation of their efficiency in low-power designs at nanometric levels. A detailed discussion of current approximate full-adder circuits implemented in CMOS technology is provided in the next two examples [8].

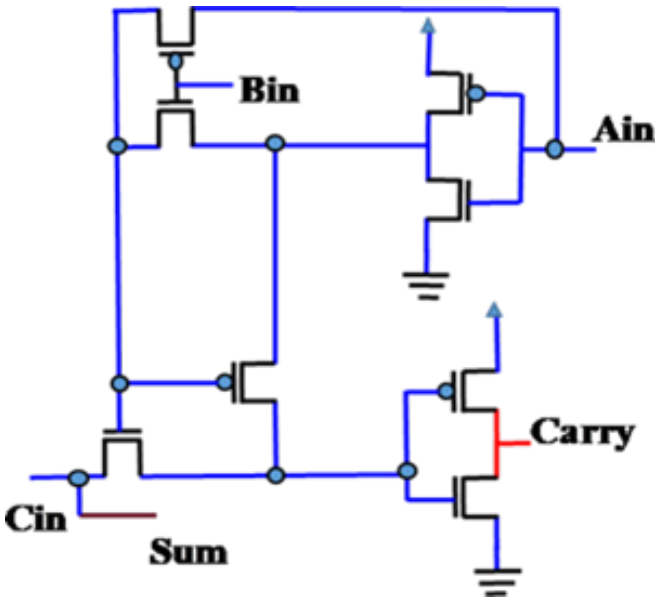
1) 9T AFA1 and 8T AFA2

Two CMOS-based approximation full adder (AFA) designs, shown in Fig. 1, are developed in the "Low-Power and Area-Efficient Approximate Full Adder for Image Processing Applications" with the goal of lowering power consumption, latency, and circuit area for error-tolerant applications such as image processing [9]. Here, approximate computation is used to trade off a tiny degree of precision for considerable gains in speed and energy economy. Power efficiency is crucial for embedded and portable devices, which are the focus of both designs [10]. The Cadence Virtuoso platform uses 90 nm CMOS technology to implement the introduced adders. Compared to traditional precise adders, the designs drastically reduce the number of transistors by improving transistor-level architecture, which lowers silicon area and dynamic power [11]. According to simulation data, both AFAs perform better in terms of Power Delay Product (PDP) since they use less power and have shorter delays than current designs [12].

While the other validated adder stresses a balanced error distribution between Sum and Carry outputs, the first adder uses a simplified carry generating process, which lowers complexity and switching activity. The AFAs' usefulness for approximation computing settings is confirmed by image processing research that shows they cause no visual distortion when used in arithmetic operations within DSP Systems [13]. The solutions maintain acceptable accuracy levels for multimedia applications while achieving significant reductions in size (up to 33%), power (up to 40%) and delay as compared to typical full adders. The paper suggests that these AFAs are promising candidates for low power VLSI systems, particularly in real-time image and video processing when minor computational errors are acceptable.



(a)



(b)

Fig. 1. (a) 9T approximate full adder (b) 8T approximate full adder

2) 14T CSOBAA & CSIBAA

In order to reduce power consumption, transistor count, and delay while maintaining acceptable accuracy, the Current Source Inverter Based Approximate Adder (CSOBAA) and the Current Sink Inverter Based Approximate Adder (CSIBAA) are two novel approximate full adder designs presented in the paper "Efficient Approximate Adders for Fast Arithmetic in Energy-Saving Applications" [14].

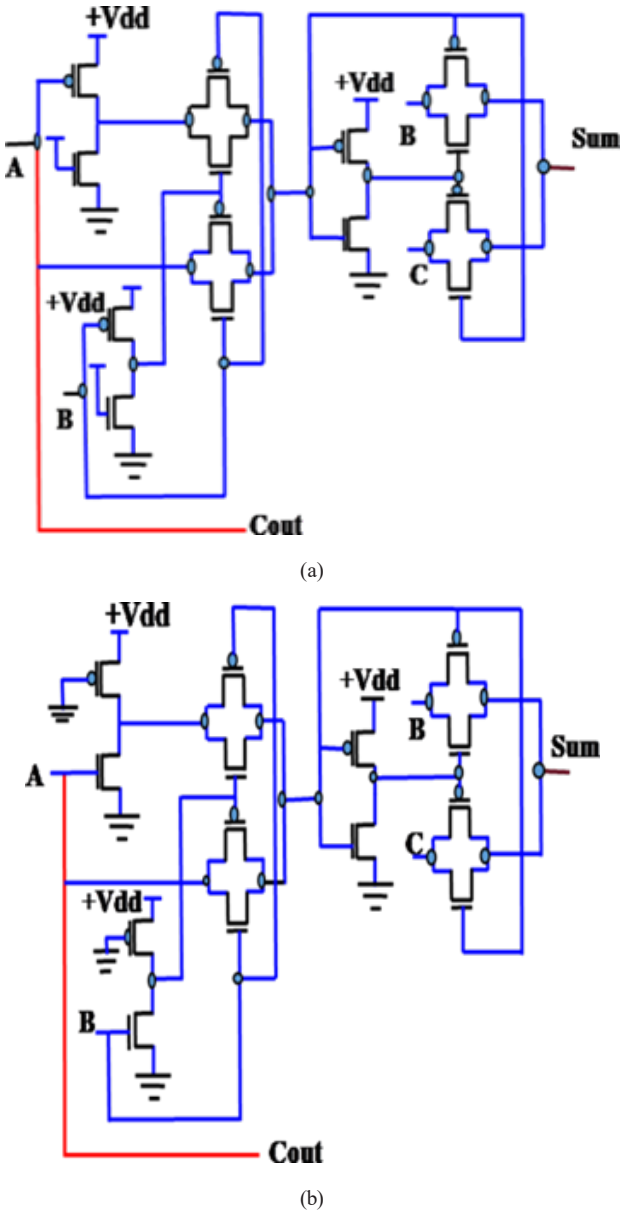


Fig. 2. (a) 14T CSOBAA (b) 14 CSIBAA

These adders, which are aimed at error-resilient applications like image and video processing, make use of approximation computing concepts, which allow for small faults in exchange for notable gains in performance and energy efficiency [15]. Both designs, as shown in Fig. 2, use only 14 transistors, which is less than many current architectures like TGA1, TGA2, and RCPFA, but they achieve similar or lower error rates when implemented in 45 nm CMOS technology using the Cadence Virtuoso tool. By connecting the carry output directly to one of the inputs, the logic complexity is decreased. The simulation findings demonstrate that the circuits have excellent temperature stability, with less than 0.00066% fluctuation from -10 °C to +100 °C, and very low power consumption (5.37nW at 0.7 V) and minimal latency (3.15ps at 1.0 V). Both sum and carry outputs attain full logic swings, and the PDP and output characteristics are constant across supply voltages [16]. These findings show that the presented AFAs are suitable for high-speed, low-power DSP and ASIC systems when a small accuracy trade-off is acceptable, eventually improving system efficiency in computationally demanding fields like multimedia.

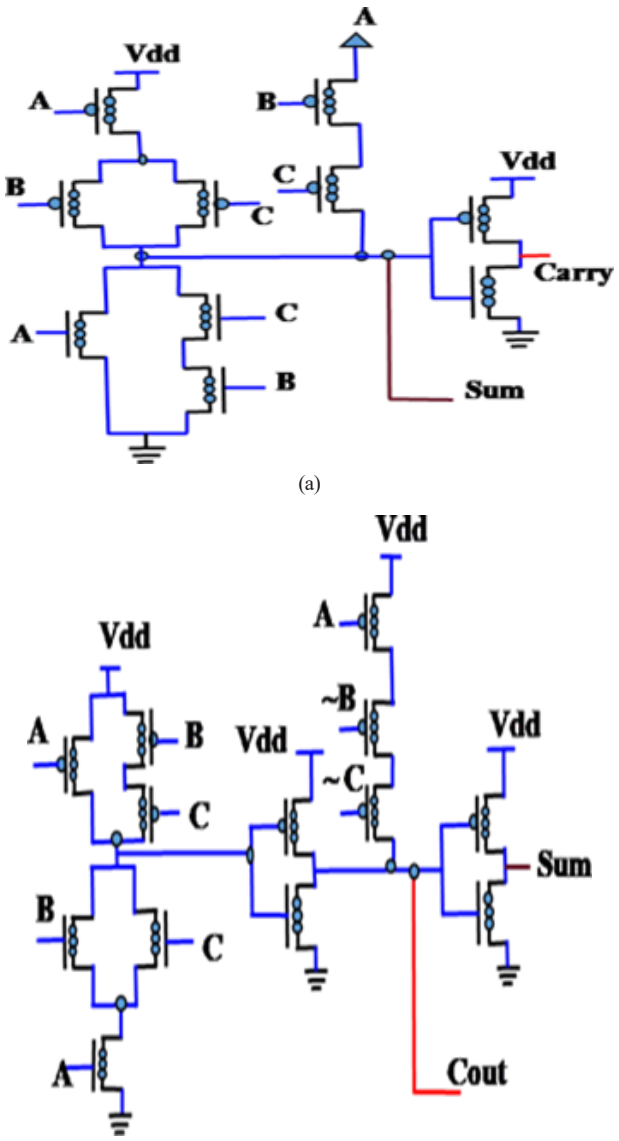
B. Emerging Nanotechnologies and CNTFET-Based Adders

CNFETs have emerged as one form of numerous device families for addressing the defects experienced in scaling CMOS devices. Strong carrier transport capability, ballistically enhanced transport, electrostatic control, and low power dissipation can all be attained in CNTFETs [17]. These devices have highly fascinated designers for implementing energy-efficient digital systems through their ability to exploit these characteristics, most commonly at nanoscale levels [18]. To exploit the benefits provided by these devices, exact and approximation- based design alternatives for full adders through CNTFETs have been developed [19]. Compared to their CMOS-based alternatives, full adders attain power-delay improvements through the 10 to 16T schemes when CNTFETs are traditionally used [20]. Lesser complexity in the logic system along with relaxed constraints in carry generation have been employed to improve efficiency in the approximation-based CNTFET adders designed. Due to the trade-off between accuracy and complexity, 6T to 12T topologies are often employed in designing the adders that include a high number of transistors, despite the fact that such designs result in extremely lower values of propagation delay along with power consumption [21]. The structure and functionality of the current approximation full adders built using CNFET technology are given in the following two examples.

1) 10T AFA1 and 13T AFA2

The "Design and Analysis of Low-Power and High- Speed Approximate Adders Using CNFETs" presents three CNFET-based approximate full adder (AFA) designs AFA1, AFA2, and AFA3 for energy-efficient and fast processing in error-tolerant applications [22]. All designs employ Pass Transistor Logic (PTL) to minimize transistor count, area, and switching activity. The adders, shown in Fig. 3, which implemented in 32nm CNFET and simulated in HSPICE at 0.9 V outperformed current designs in terms of PDP, delay, and power. The AA1 uses 8 transistors with 14 Sum and 1 Carry error, resulting in the optimum accuracy-power trade-off. AA2 similarly has eight transistors, but with one sum and three carry faults, which reduces power even further. The AA3 employs power even further. The AA3 employs 6-8 transistors with greater error rates but the smallest

size and power. Image processing studies demonstrate low quality loss for AA1 and AA2, with tolerable deterioration for AA3 in tolerant scenarios [23]. These CNFET PTL-based AFAs offer a configurable balance of accuracy, speed, and energy efficiency for multimedia, DSP, and real-time low-power systems



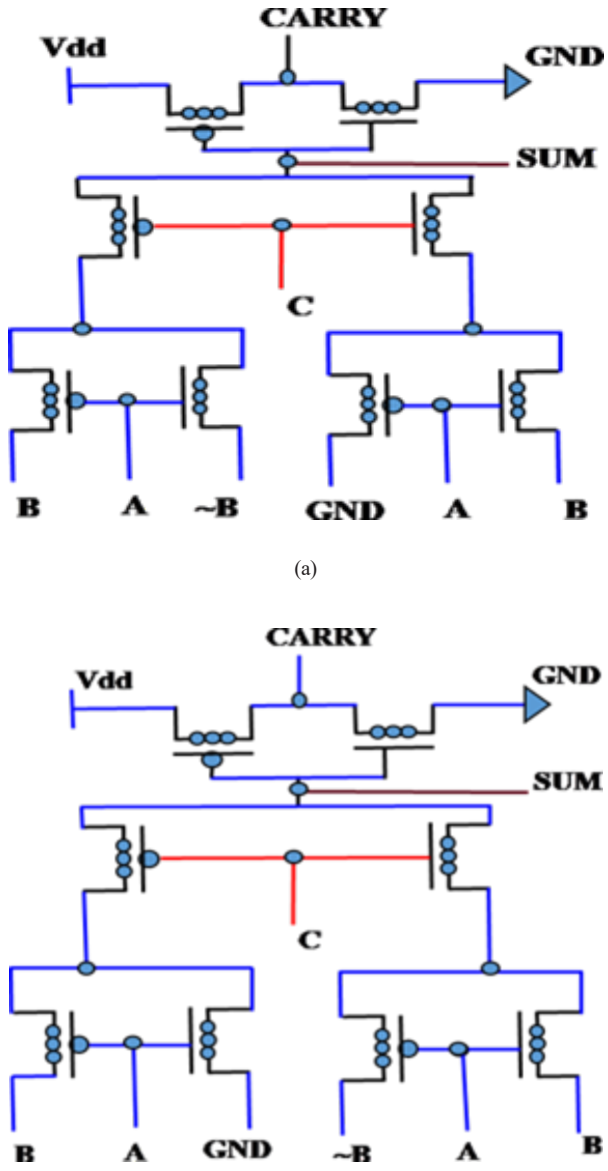
(a)

(b)

Fig. 3. (a)10T approximate full adder (b)13T approximate full adder

2) 8T PTL AFA1 & AFA2

Two new approximate full adders shown in Fig. 4, designed for low power, low delay, and high efficiency in 32 nm CNTFET technology are presented in the publication "Approximate Full Adders Design for Energy Efficiency using CNTFETs" [24]. The demand for energy-efficient circuits in portable, error-tolerant applications like image and video processing where precise accuracy is not essential serves as the driving force. Because of their configurable threshold voltage, low power dissipation, and faster switching speed, CNTFETs are preferred over MOSFETs. To reduce the number of transistors and increase speed, both introduced systems make use of PTL [25]. While the second adder requires just eight transistors and has one error in Sum and three in Carry, the first adder has one error in both Sum and Carry [26]. The first adder outperforms current 10-transistor designs with a PDP of 0.095082 aJ while the second achieves 0.113396 aJ when simulated in Cadence Virtuoso at 0.9 V. Compared to earlier work, the delay values are around 1.495 ns, and the power usage is much lower. In order to increase computing speed and lower PDP, the adders were also incorporated into a 2x4 multiplier, taking the place of traditional adders in the first adder has one error in both Sum and Carry [27]. The first adder outperforms current 10-transistor designs with a PDP of 0.095082 aJ while the second achieves 0.113396 aJ. When simulated in Cadence Virtuoso at 0.9 V. Compared to



(a)

(b)

Fig. 4. 8T CNTFET-based approximate adders

earlier work, the delay values are around 1.495 ns, and the power usage is much lower [28]. In order to increase computing speed and lower PDP, the adders were also incorporated into a 2x4 multiplier, taking the place of traditional adders in the architecture. The first presented adder's low PDP, low delay, and small space make it especially well-suited for approximation computation, according to simulation data. All things considered, the designs show that CNTFET-based approximation adders can successfully improve VLSI system performance and energy economy, particularly for DSP and multimedia applications where a low level of error tolerance is acceptable [29].

C. Ultra-Low-Complexity Approximate Adder Designs

More aggressive approximation approaches implemented at the transistor level are the focus of new research on the design of ultra-low complexity approximate adder architectures. Such approaches often lead to a reduction or removal of carry chains, which results in a significant decrease in switching activity and transistors. While the presented approaches offer a considerable reduction in terms of power, they also result in an error. If the error factor is not taken into consideration in the developed approach, it can affect the overall computing environment. Approximate adders with a low transistor budget that utilize a mix of Pass Transistor and Logic styles are discussed in a number of research papers. However, the overall resilience of the introduced approach may decrease with changes in the temperature and voltages. In summary, an attempt at designing an ultra-minimal adder with a fair level of Computing accuracy and signal integrity remains a research challenge.

D. Approximate Computing in Image and Edge Processing Applications

A large number of applications related to image processing like feature detection, edge detection, image filtering, etc., used the technique of approximate addition. Based on the details gained from the experiments, the applications can withstand some arithmetic approximations with minimal deterioration in the quality of the generated image. Measures used to determine the effect of approximation are often the overall image quality, the precision in the detection of edges, structural similarity, and the peak value in the signal-to-noise ratio. Notably, the general application of approximate arithmetic units can greatly assist with the energy requirements related to the application of edge computing with minimal rates of power consumption. A large proportion of existing approximate adder designs are mainly validated on the circuit level with minimal implementation on application-driven validation, mainly on those applications related to image processing on the edges [30].

E Research Gap and Motivation

There has been little work on ultra-small designs including the highly specific 3T design for real-time computation of edge image processing applications, although great progress has been observed in the design of CNTFET-based approximate adders in the field of approximate computing. These AFAs have either largely been centered on power savings while ignoring the applications or have focused on the accuracy of the AFA design while employing a considerable number of transistors in the design. Moreover, the energy/accuracy balance in the context of

TABLE I
COMPARISON OF APPROXIMATE FULL ADDER ARCHITECTURES

Supply Voltage	Design	Power(μw)	Delay(ps)	PDP($J\times10^{-17}$)	EDP($Js\times10^{-29}$)	Transistor Count
Vdd = 1V	[32]	1.5892	21.572	3.4283	73.9552	12
	[33]	5.6395	15.429	8.7013	134.253	13
	[34]	5.6500	13.640	7.7068	105.120	9
	[35]	1.3531	15.943	2.1572	34.3922	8
	[36]	1.3726	18.951	2.6013	49.2972	9
	[37]	5.9624	13.223	7.8839	104.248	15
	[38]	1.3203	13.354	1.7631	23.5444	8
	[39]	1.8662	13.604	2.5388	34.5380	10
	[40]	1.4943	11.002	1.6440	18.0871	14
	[Proposed]	0.8332	2.7787	0.2315	0.64326	3
Vdd = 0.9 V	[32]	1.1118	23.207	2.5801	59.8763	12
	[33]	3.2248	16.358	5.2753	86.2933	13
	[34]	3.2707	13.725	4.4891	61.6128	9
	[35]	0.94111	16.814	1.5824	26.6064	8
	[36]	0.96632	19.395	1.8742	36.3501	9
	[37]	3.4730	14.550	5.0531	73.5226	15
	[38]	0.9674	13.701	1.3255	18.1606	8
	[39]	1.3423	16.265	2.1832	35.5105	10
	[40]	0.9989	11.431	1.1419	13.0527	14
	[Proposed]	0.5848	4.6207	0.2702	1.24851	3

real- time applications of edge computing has been explored in a very little number of prior studies within the design of AFAs. This has led to the idea presented in this manuscript on the design of a low power approximation full adder based on CNTFET devices while demonstrating the reduced hardware complexity along with the required degree of computation precision in real-time edge image processing applications [31]. The comparison of some of the existing Approximate Full Adder Architectures is shown in Table I.

III. Proposed Design

The proposed 3T AFA design and behavior are presented in this part, along with how it can be integrated into a hardware- efficient object identification pipeline for edge-based image processing applications. A. 3-T AFA Design by taking use of imprecise logic approximations, the introduced full adder greatly reduces the number of transistors and logic. Our solution generates approximate sum and carry output using only three transistors, in contrast to traditional full adders that require 28 or more transistors to attain full logic precision. The Truth Table of the Proposed 3T Approximate Full Adder is given in Table II.

Table II
Truth table for 3T Approximate Full Adder

A	B	C (Cin)	Exact Sum	Exact Cout	Approx Sum	Approx Cout
0	0	0	0	0	0	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	1	0
1	0	0	1	0	1	1
1	0	1	0	1	1	1
1	1	0	0	1	1	1
1	1	1	1	1	1	1

A. Presented 3T Approximate Full Adder Design

By taking use of imprecise logic approximations, the designed full adder greatly reduces the number of transistors and logic. Our solution generates approximate sum and carry-output as shown in Fig. 5 using only three transistors, in contrast to traditional full adders that require 28 or more transistors to attain full logic precision.

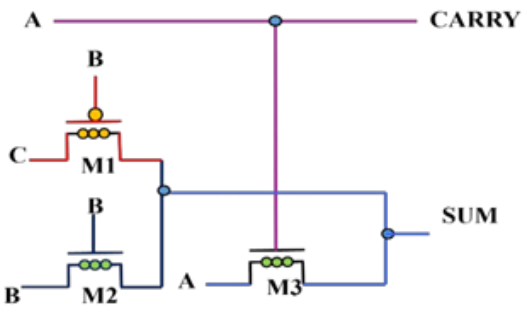


Fig. 5. Proposed 3T approximate full adder

B. Logic Expressions of the Proposed 3T Approximate Full Adder

The following approximate logic equations control the developed adder's functional behavior:

1) Carry Generation: Input A is the immediate source of the carry output:

$$\text{Carryout} = A \tag{1}$$

2) Sum Generation: The approximate sum output is as follows:

$$\text{Sum} = A|(B\&\sim C)|C \tag{2}$$

This expression does involve B and Cin (C), so the original sentence does not accurately describe the sum logic. transistors count while preserving adequate accuracy. Although, "The sum logic does not require the entire XOR logic is usually needed in accurate full adders because it considers all three inputs (A, B, and Cin) in a simplified Boolean the logic operation is not entirely accuracy-based, it offers a quick and portable solution that works well for image processing applications when perfect accuracy is not required. These formulas work together to enable the adder to function with only three transistors, providing great compactness, low delay, and low power consumption—all of which are essential for edge-based real time vision systems.

C. Trade-Off:

Although this approximation greatly lowers size, latency, and power consumption, it causes a small logic error in some input combinations. By doing away with intricate gate architectures, this method drastically lowers hardware overhead.

D. Object Detection:

This approximation full adder is ideal for pixel-level operations like convolution layers and pre-processing. Because object identification algorithms (particularly lightweight ones) can tolerate minor numerical mistakes, this AFA can replace typical FAs in accumulation circuits within CNNs or filters.

IV. Results And Discussion

To prove the suitability of the novel PTL-based CNFET 3T approximation full adder circuit for real-time edge image processing tasks, its performance is thoroughly evaluated and compared with many state-of-the-art approximate adder circuits [41]. The presented 3T CNFET approximate full adder based on PTL for ultra-low power and area is shown in Fig. 5. The output waveforms for the new design are shown in Fig. 6, ensuring correct functional operation with an appropriate approximation for error-tolerant image processing tasks [42]. To analyze the energy efficiency, delay performance, and voltage scalability of the circuit in low-power operating conditions, simulations are conducted under the same conditions at lower supply voltages of Vdd = 1V and 0.9 V. The introduced PTL-based CNFET circuit consistently provides better performance than the existing approximate full-adder circuits in several key performance aspects, such as average power dissipation, propagation delay,

PDP, EDP, and transistor count. The introduced adder circuit consumes an ultra-low power of 0.8332 µW at Vdd = 1V, which is significantly lower than that of all other compared circuits [43]. This improvement is mainly attributed to the joint advantages of the PTL-based ultra- minimal 3T structure and the excellent electrical properties of CNFET technology, including near-ballistic transport, low leakage current, and enhanced electrostatic control. Despite the presence of a propagation delay of 2.7787ps, the circuit exhibits the lowest PDP value of 0.2315×10^{-17} J and EDP value of 0.64326×10^{-29} J·s, which is a clear indication of its superior energy efficiency. When the supply voltage is lowered to 0.9V, the power dissipation reduces to 0.5848µW, which is a clear indication of its superior low-voltage performance [44]. However, the resulting delay is increased to 4.6207 ps, which is still within acceptable limits for error- tolerant edge image processing tasks. The new adder circuit exhibits the lowest PDP value of 0.2702×10^{-17} J and EDP value of 1.24851×10^{-29} J·s compared to the existing CMOS- and CNFET-based approximate adder circuits, including those designed at lower voltages. Additionally, the introduced PTL-based circuit requires only three transistors, contrary to the 8-15 transistors used in previous approaches, which clearly indicates its superior silicon area, parasitic capacitance, and Owing to the inherent robustness of edge image processing methods such as edge detection and feature extraction to errors, the minute errors caused by the approximation have no effect on the quality of the image. From the results, it is clear that the recommended PTL-based 3T CNFET approximate full adder circuit offers a remarkable balance between power efficiency, delay, and hardware complexity, thus emerging as a promising solution for edge image processing systems conditions at lower voltages of Vdd =1V, Vdd = 0.9V. The introduced PTL-based CNFET circuit consistently provides better performance than the existing approximate full adder circuits in several key performance aspects, such as average power dissipation, propagation delay, PDP, EDP, and transistor count, as depicted in Table III.

TABLE III
SIMULATION AGAINST 0.9V AND 1V VDD OF PROPOSED APPROXIMATE FULL ADDER

Supply Voltage (Vdd)	Proposed Design	Power(µw)	Delay(ps)	PDP($J\times10^{-17}$)	EDP($Js\times10^{-29}$)
0.9V	3Transistor	0.5848	4.6207	0.2702	1.24851
1V	3Transistor	0.8332	2.7787	0.2315	0.64326

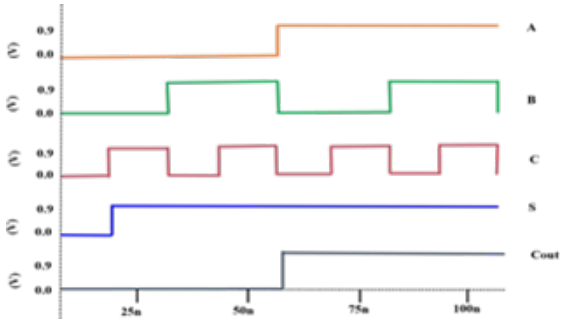


Fig. 6. Output Waveforms for Proposed 3T Approximate full adder

The introduced adder circuit consumes an ultra-low power of 0.8332 µW at Vdd = 1V, which is significantly lower than that of all other compared circuits [43]. This improvement is mainly attributed to the joint advantages of the PTL-based ultra-minimal 3T structure and the excellent electrical properties of CNFET technology, including near-ballistic transport, low leakage current and enhanced electrostatic control. Despite the presence of a propagation delay of 2.7787ps, the circuit exhibits the lowest PDP value of 0.2315×10^{-17} J and EDP value of 0.64326×10^{-29} J·s, which is a clear indication of its superior energy efficiency. When the supply voltage is lowered to 0.9V, the power dissipation reduces to 0.5848µW, which is a clear indication of its superior low-voltage performance [44]. However, the resulting delay is increased to 4.6207 ps, which is still within acceptable limits for error- tolerant edge image processing tasks. The new adder circuit exhibits the lowest PDP value of 0.2702×10^{-17} J and EDP value of 1.24851×10^{-29} J·s compared to existing CMOS- and CNFET-based approximate adder circuits, which including those designed at lower voltages. Additionally, the introduced PTL-based circuit requires only three transistors, contrary to the 8-15 transistors used in previous approaches, which clearly indicates its superior silicon area, parasitic capacitance, and Owing to the inherent robustness of edge image processing methods such as edge detection and feature extraction to errors, the minute errors caused by the approximation have no effect on the quality of the image. From the results, it is clear that the recommended PTL-based 3T CNFET approximate full-adder circuit offers a remarkable balance between power efficiency, delay, and hardware complexity, thus emerging as a promising solution for edge image processing systems.

The presented PTL-based 3-transistor CNFET approximate full-adder's physical layout presented in Fig.7, has also been carefully sketched and developed to verify the new design's feasibility for hardware realization. The highly compact nature of the introduced design is also evident in the layout, which further

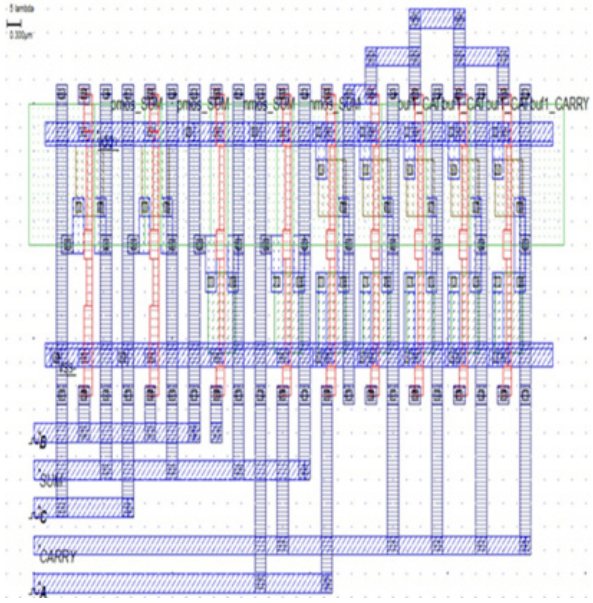
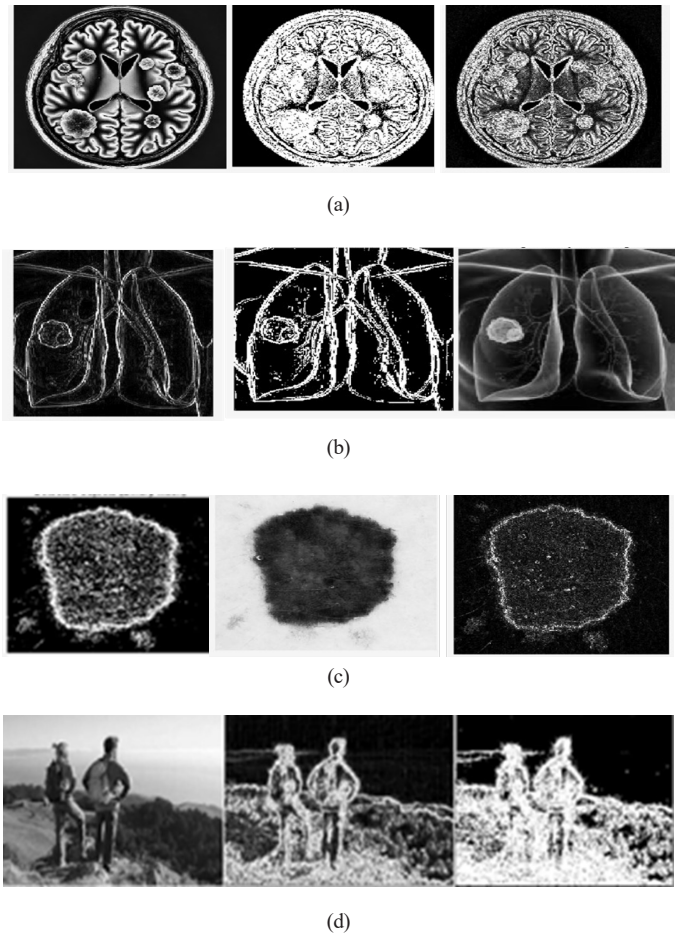


Fig. 7. Layout of the Proposed 3T Approximate Full Adder

has less parasitic capacitance and routing complexity, both of which reduce power consumption and enhance energy efficiency. The recommended adder's viability for high-density integration in image processing data paths, where area and power constraints are significant, is further evident from the compact layout.

V. Image Processing Application Of Presented Approximate Full Adder

The recommended PTL-based 3T CNFET approximate full adder is incorporated into a real-time edge image processing system to demonstrate its utility. As edge detection is a computationally intensive but robust task, approximate arithmetic architectures emphasizing simplicity and low power consumption are appropriate in this context. The qualitative results for the natural scene image and medical image datasets are presented in Fig. 8. The natural image illustrates a general-purpose grayscale scene, while the evaluated medical datasets include images of skin cancer, lung cancer, and brain tumors (MRI and CT scans). The original grayscale image, the gradient magnitude image derived using the introduced approximate adder, and the final object detection (binary mask) are presented for each dataset [45]. Although the ultra-minimal 3T approximate arithmetic cell is employed, the visual outcome unequivocally indicates that the principal edges and boundaries are preserved for all datasets.



(a)

(b)

(c)

(d)

Fig. 8. Object detection results using gradient magnitude Analysis
(a). (i) Original Gray Scale Image (ii) Gradient Magnitude
(iii) Detected Object images of Brain Tumor Dataset (MRI Scans)
(b). (i) Original Gray Scale Image (ii) Gradient Magnitude
(iii) Detected Object images of lung cancer dataset
(c). (i) Original Gray Scale Image (ii) Gradient Magnitude
(iii) Detected Object images of Skin Cancer
(d). (i) Original Gray Scale Image (ii) Gradient Magnitude
(iii) Detected Object images of Natural Scene Image

Table IV. presents a summary of the quantitative analysis using the Structural Similarity Index Measure (SSIM) and Peak Signal-to-Noise Ratio (PSNR). As observed, the SSIM values lie between 0.23 and 0.31 for different types of images, while the PSNR values vary from 3.69 dB to 8.82 dB. These values are sufficient for edge detection applications, where the perceived accuracy and continuity of structure are more significant than the pixel accuracy, although they are less than those calculated using exact arithmetic units.

The usefulness of the presented adder in the healthcare-focused image analysis is confirmed by the fact that medical images preserve diagnostically significant edge information, such as tumor boundaries and tissue patterns. The purposeful approximation of the 3T PTL-based CNFET design, which significantly reduces the number of transistors, switching activity, and power dissipation, is the reason for the comparatively lower PSNR and SSIM values. In real-time edge image processing applications, this approximation is acceptable, especially in resource-constrained environments such as portable medical equipment and edge computing systems. In general, the results clearly demonstrate that the introduced 3T CNFET approximate full adder provides substantial improvements in hardware complexity and power dissipation while facilitating effective edge detection for different types of images, including medical and also natural images. In low-power real-time image processing systems, the new architecture is a feasible alternative. unless it is necessary for the true interpretation of your figures.

Table IV
PSNR and SSIM Evaluation on Benchmark Image Datasets

Dataset	PSNR (dB)	SSIM
Brain Tumor	7.13	**0.25348**
Lung Cancer	8.82	**0.31313**
Skin Cancer	5.61	**0.26363**
Natural Scene Image	3.6907	**0.23436**

VII. Conclusion

To address the real-time edge image processing task, this work presents an ultra-low power 3T approximate full adder designed using PTL technology with CNFETs. Compared to the existing approximate adders, the developed design adder significantly reduces the number of transistors and the complexity of the circuit, resulting in a substantial reduction in power consumption, delay, and energy efficiency. The new adder's tolerance to low-voltage conditions is validated through circuit-level simulations performed at 1 V and 0.9 V supply voltages [46]. The presented adder is integrated into a gradient-based edge de-

tection system and tested on different types of images, including medical images (brain tumor, lung cancer, and skin cancer image datasets) and a natural scene image, to validate the application-level performance. The essential edge and structural details are preserved despite the approximation process, as validated through qualitative and quantitative analysis. For error-tolerant image processing tasks, the achieved PSNR and SSIM results demonstrate sufficient perceptual quality. The introduced PTL-CNFET 3T approximate full adder is an excellent choice for low-power, real-time image processing and edge computing tasks due to its efficient trade-off between accuracy and energy efficiency.

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