Variation Tolerant SRAM with Enhanced Stability for Wearable Healthcare Devices

M.Kavitha, S.Ramani, and P.K.Janani

***Abstract*—As technology scales down CNTFET (Carbon Nano Tube Field Effect Transistor) circuits has gained importance in VLSI design due to exacerbation of process parameter variations in CMOS. Particularly design of SRAM cell needs more attention as it occupies the larger space in CPU of the battery powered wearable devices. Hence it is a challenging task to the chip designer because the power, energy, speed and stability of the memory cell has a greater impact on system CPU efficiency. A variation tolerant nine transistor CNTFET SRAM cell is proposed in this work. Metrics considered for investigating the proposed SRAM performance is power, delay, power delay product (PDP) and static noise margin (SNM). Stanford University 32 nm CNTFET model and HSPICE tool is utilised for the simulation. In proposed SRAM the read and write power reduction is improved by 4.7x and 9.9x respectively, while the read delay and PDP reduction is improved by 10x than conventional SRAM. The hold, read and write stability of proposed memory cell is enhanced by 1.4x, 1.2x and 4.1x respectively compared to conventional structure.**

***Index Terms*—VLSI, SRAM, Low power, Stability, Delay, PDP.**

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I. Introduction

Embedded memory systems influence the overall performance, efficiency and cost of CPU of modern-day applications. Key design parameters to design an improved SRAM vary according to applications. For modern artificial neural networks, graphics processors, servers etc, high performance is of highest priority than energy [1]. Applications like image processing, Internet of Things (IoT), wearable devices demand reliability, stability and energy efficiency [2]. Wearable devices have occupied a significant place in health monitoring as they help the patients to self-monitor their health conditions. Few examples are wearable fitness trackers and smart health watches, help to track the patient's physical activity and heart rate as they are equipped with sensors synced to their smart phones. Wearable ECG monitors help to measure electrocardiograms and blood pressure and other vitals. The most commonly used device is the wearable blood pressure monitor which, apart from measuring blood pressure, also indicates the calories burnt which help the patients to maintain their health condition under control. Wearable devices in medical field demand ultra-low power and robust SRAM to extend the device battery life and to get reliable results respectively [3]-[5]. CNTFET is the future alternative of MOSFET circuit designs. With respect to carrier mobility, scalability, short channel effects etc, CNTFET performance is better than its CMOS counterpart. Semiconducting channel in MOSFET is replaced with cylinder shaped carbon nano tubes (CNT) tubes. CNT tubes function as semiconductor or metallic depending on the chirality vector. Number of CNT tubes used in the channel region, diameter of CNT tubes, chirality, pitch, gate dielectric, oxide thickness etc. has a greater impact on CNTFET characteristics [6]-[9].

Conventional 6T SRAM has four transistors in cross coupled inverter for storing one bit data and two write access transistors to enable write operation [10]. Read stability of the conventional 6T SRAM is improved by adding a read port. Additional read port provides a separate path for read operation and isolates the storage nodes from bit lines during read operation to increase the read stability [11]. By sharing write bit line and read bit lines in a column, a low power and high stable 9T SRAM can be realized since separate write word lines and drivers improve the write stability, and a dedicated read access transistor along with read control transistor improves the read stability [12]. 9T SRAM with supply feedback minimizes power. A P-type transistor is employed between the supply and load transistors and connecting its gate to the storage node. This feedback makes the cell flip even with strong load transistors by weakening the pull up path [13]. Power gating the SRAM circuit decreases its power consumption and improves stability. Power gating structure puts the SRAM in sleep, drowsy and active mode depending on the control signals [14]-[15].

9T SRAM with read control signal has 6T SRAM cell in upper sub circuit while the lower sub circuit comprises of read circuitry with bit line access transistors along with read access transistor. Read access transistor is enabled by RD signal during read operation and it is disabled during write operation. Due to separate read circuit, the data stability of this SRAM is increased [16]. 9T SRAM with separate read buffer provides read disturb free operation as the read path is decoupled from the storage nodes which improve the stability of the memory cell [17]. Conventional asymmetrical nine transistor SRAM (CA9T

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SRAM) given in Fig. 1 improves the read and write stability. Read stability is improved by the read buffer (M8 and M9) by isolating the storage nodes from bit lines while the writing ability is increased by the write assist transistor M7 [18]. In this paper a low power, high speed CNTFET based SRAM with enhanced write stability is presented and its performance is compared with conventional structure shown in Fig. 1.

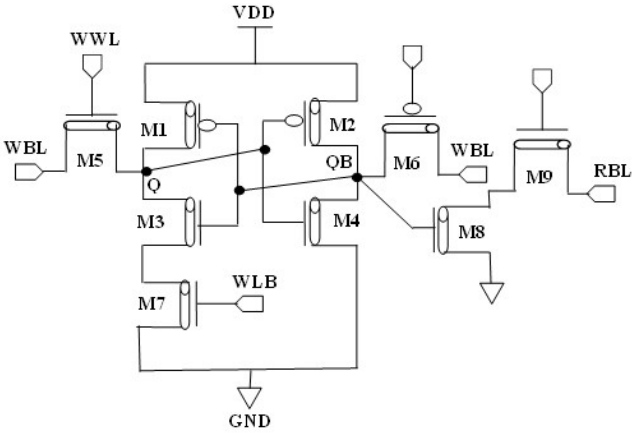


Fig. 1. CA9T SRAM Cell

II. Proposed SRAM Structure

The proposed asymmetrical nine transistor CNTFET SRAM (PA9T SRAM) with enhanced stability is depicted in Fig. 2. PA9T SRAM incorporates two techniques for minimizing power, namely stack and multi-threshold voltage technique. Transistors in cross coupled inverters (M1, M2, M3 and M4) are designed as high threshold transistors (HVT) according to (1).

$$V_{th} = \frac{0.43}{D_{CNT}(nm)} \tag{1}$$

where V_{th} - CNTFET threshold voltage and D_{CNT} -CNT tube diameter [7]. Transistors M6, M7, M8 and M9 are designed as low voltage transistors (LVT). Advantage of utilizing both LVT and HVT in circuit design is that it suppresses power consumption and improves stability without increasing the layout area. Transistor M8 and M9 are the read bit line access transistor and read transistor respectively. The HVT sleep transistor (NS) at the source of the read transistor alleviates the read bit line leakage during idle states. The sleep transistor is connected to all the sources of the read transistors i.e NS is shared by all the read transistors in the SRAM array.

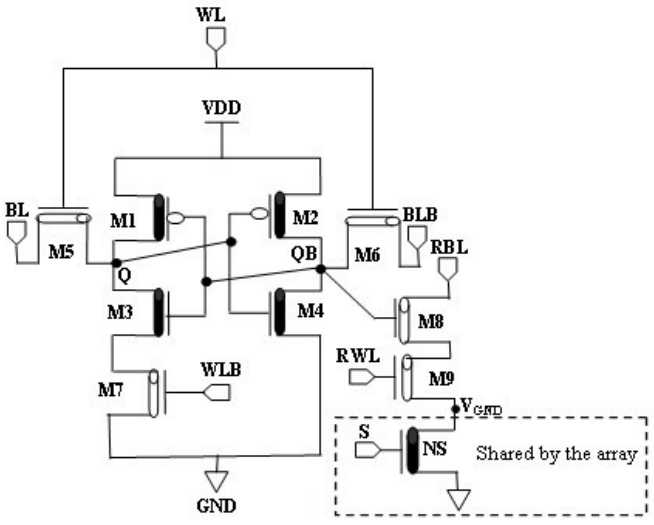


Fig. 2. PA9T SRAM Cell

Fig. 3 reveals that the proposed SRAM has a natural stacking effect, i.e the transistor M9 gets naturally stacked with the sleep transistor NS. Stacking effect reduces the currents through stacked pair transistors if more than one transistor is turned '*off*' [19]. Equations (1) to (8) prove the effect of stacking transistors on leakage. Let I_{off} is the subthreshold current with $V_{GS} = V_{BS} = 0$, $V_{DS} = V_{DD}$, and if $V_{DS} > 3kT/q$, the MOS transistor leakage is

$$I_{leak} = I_{off} 10^{-\frac{1}{S}[\Delta V_G + \lambda_d \Delta V_D + k_\gamma \Delta V_B]} \tag{2}$$

where S - subthreshold swing, λ_d - DIBL factor and k_γ- body effect co-efficient. Referring (2) the leakage of M9 and NS can be written as

$$I_{stack-M9} = W_9 I_{off} 10^{\frac{-(1+\lambda_d+k_\gamma)V_X}{S}} \tag{3}$$

$$I_{stack-NS} = W_{NS} I_{off} 10^{\frac{-\lambda_d(V_{DD}-V_X)}{S}} \tag{4}$$

where W_9, W_{NS}- width of the transistors M9 and NS respectively.

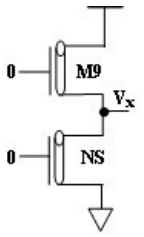


Fig. 3. Transistor Stack

The intermediate node voltage V_x reaches an equilibrium level when the leakage through M9 and NS are equal, and it can be determined from (3) and (4).

$$V_x = \frac{\lambda_d V_{DD} + S \log \frac{W_9}{W_{NS}}}{1 + k_\gamma + 2\lambda_d} \tag{5}$$

$k_\gamma << 1+2\lambda_d$ in short channel devices and hence (5) becomes

$$V_x \approx \frac{\lambda_d V_{DD} + S \log \frac{W_9}{W_{NS}}}{1 + 2\lambda_d} \tag{6}$$

Leakage in stacked M_9 and NS is found by substituting V_x in either (3) or (4).

$$I_{stack} = {W_9}^{\alpha}{W_{NS}}^{1-\alpha} I_1 10^{\frac{-\lambda_d V_{DD}}{S}(1-\alpha)} \quad (7)$$

where $\alpha = \frac{\lambda_d}{1+2\lambda_d}$. Leakage reduction in transistor stack with widths W_9 and W_{NS} with respect to a single transistor with width 'W' is

$$X = \frac{I_{single}}{I_{stack}} = \frac{W}{{W_9}^{\alpha}{W_{NS}}^{1-\alpha}} 10^{\frac{\lambda_d V_{DD}}{S}(1-\alpha)} \quad (8)$$

When W_9=W_{NS}=W, the stack factor X can be written as

$$X = 10^{\frac{\lambda_d V_{DD}}{S}(1-\alpha)}, \text{ Or } \quad X = 10^{\frac{\lambda_d V_{DD}}{S}\left(\frac{1+\lambda_d}{1+2\lambda_d}\right)} = 10^{U} \quad (9)$$

where *'U'*- universal stack exponent of two transistors. It is apparent from (9) that leakage is greatly reduced in stacked transistors compared to a single transistor. Equations (2) to (9) are applicable to CNFETs also, hence proving the stacking has considerable effect in CNFET circuits also [20]-[21]. Hence the proposed SRAM can provide high power reduction due to stacking effect as well as the multi-threshold voltage design.

PA9T SRAM supports single ended read operation. RBL is charged to VDD prior to read operation and then the read control signal RWL is asserted to read the data in storage nodes. The word line WL and sleep signal 'S' are maintained at 0V and VDD respectively. In case if '1' is stored at QB, RBL gets discharged through the read port (M8, M9 and sleep transistor NS). Alternatively, if the data at QB is '0', then RBL is maintained at VDD level due to the absence of discharge path. Read stability is improved in this structure as the data is isolated from the bit lines as well as the source of M9 are maintained at ~0V.

PA9T SRAM provides double ended write operation, wherein the bit lines BL and BLB are charged to VDD and 0V respectively in order to write '1' at the storage node Q. Read word line RWL and sleep signal are maintained at 0V and VDD respectively. Data '1' is forced from the bit line BL to the node Q through the write access transistor M5. To write '0', BL is maintained at 0V while BLB is held at VDD. During this operation, the contention current of M3 is eliminated as the transistor M7 is in 'off' condition. Write stability is improved by the HVT cross coupled inverters without compromising layout area. In sleep or hold mode, word control line WL, read control line RWL, and sleep signal 'S' are maintained at 0V. Sleep transistor NS is cutoff to minimize read bit line leakage as the transistors M8, M9 and NS form stacked pair. Further the cell leakage current is reduced due to the usage of high threshold voltage transistors in cross coupled inverters. Since the source of M3 is at level ~0V, cross coupled inverters experience almost full supply voltage which enhances hold stability.

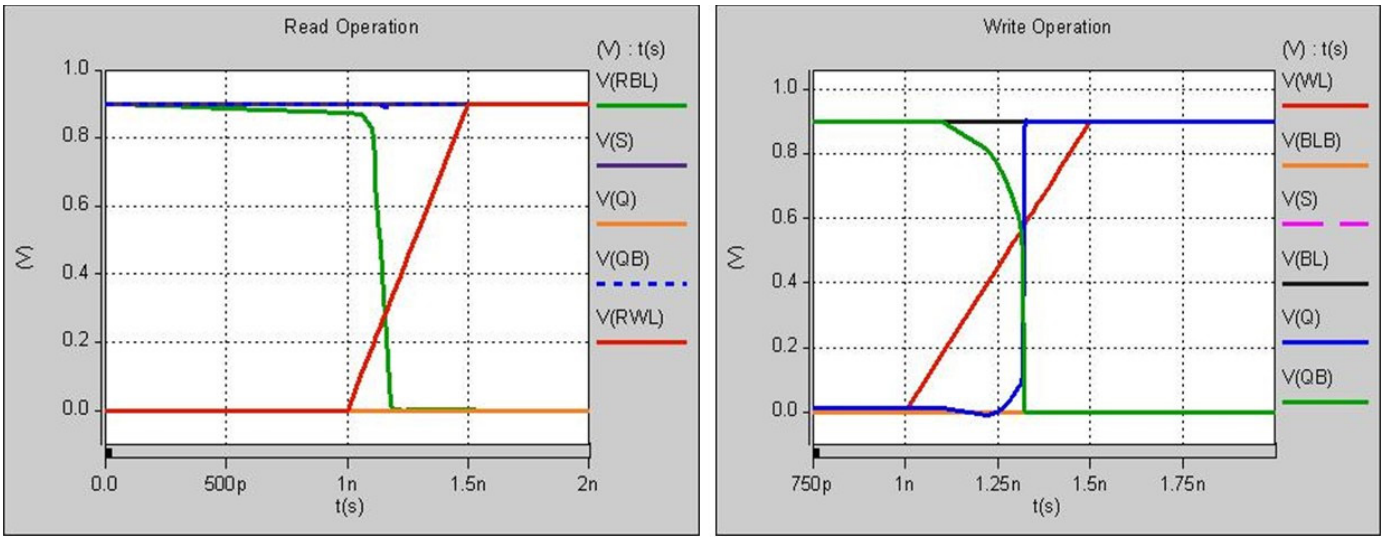
III. Results and Discussion

Stanford University CNTFET model and HSPICE is used to simulate the conventional and proposed SRAMs. Parameters used for SRAM cell design are:

- Channel length of both CNTFETs: 32nm
- Temperature: 27°C
- CNT channel mean free path (L_{geff}): 100nm
- Coupling capacitance (C_{sub}): 40pF/m

Influence of nanoarray pitch, gate dielectric, number of CNT tubes used in CNTFET, supply voltage on the performance of CA9T SRAM and PA9T SRAM is analyzed. Metrics considered for investigating the performance of CA9T SRAM and PA9T SRAM are hold, read and write power, read and write delay, power delay product (PDP) and SNM. Conventional and proposed asymmetrical SRAM structures are maintained in hold, read and write modes as discussed in Section II to evaluate these metrics.

The states of various nodes in proposed PA9T SRAM during read and write modes are provided in Fig. 4. Figs. 5 to 8 reveals the effect of CNFET parameters on power and delay of



(a) (b)

Fig. 4. PA9T SRAM various node states in (a) Read operation (b) Write operation

CA9T SRAM and PA9T SRAM. In hold mode, the SRAM is in data retention state, and no control signal is asserted. The power consumption in this mode is mainly due to leakage of the cross coupled inverters, write access transistors and read port transistors. As threshold voltage increases, power decreases hence leakage in cross coupled inverters is mitigated as it contains high threshold voltage transistors. Also, as the sleep transistor is in 'off' state and the source of the read port transistor M9 is maintained at VGND that is at a level higher than the ground level leading to leakage power minimization. Addition of the sleep transistor NS does not increase the layout area as it is shared by all the read ports in SRAM array, but it contributes a lot in leakage reduction in hold mode. Read power is reduced in PA9T SRAM because the 'on' sleep transistor raises the source level of the read transistor M8 and read operation is also faster than CA9T SRAM. Write access transistor is turned 'off' and the source of M3 is at potential greater than ground level, which aids in writing the data into the storage node Q quickly. The write power and write delay is low compared to conventional CA9T SRAM.

Dependence of leakage power and dynamic power on supply voltage of CMOS VLSI circuits is given by (10) and (11) respectively.

$$P_{leak} \propto I_{leak} V_{DD} \tag{10}$$

$$P_{dynamic} = C_L V_{DD}^2 f \tag{11}$$

where C_L - load capacitance, V_{DD} - supply voltage and f - switching frequency [10]. The gate delay is

$$T_{\mathrm{pd}} \alpha \frac{C_L V_{\mathrm{DD}}}{I_{\mathrm{DS}}} \tag{12}$$

where V_{th} - threshold voltage, and I_{DS} - drain to source current [10]. Simulation results in Fig. 5 confirm the above equations that as supply voltage increase leakage, dynamic power and delay increase.

When pitch is varied, the inner tube spacing between the consecutive tubes gets varied. According to (13), increasing the pitch raises the gate width, and gate width is inversely proportional to 'on' resistance. So, increasing the pitch increases power consumption and on contrary minimizes delay as shown in Fig. 6.

$$W_G = max(W_{min}, N * S) \tag{13}$$

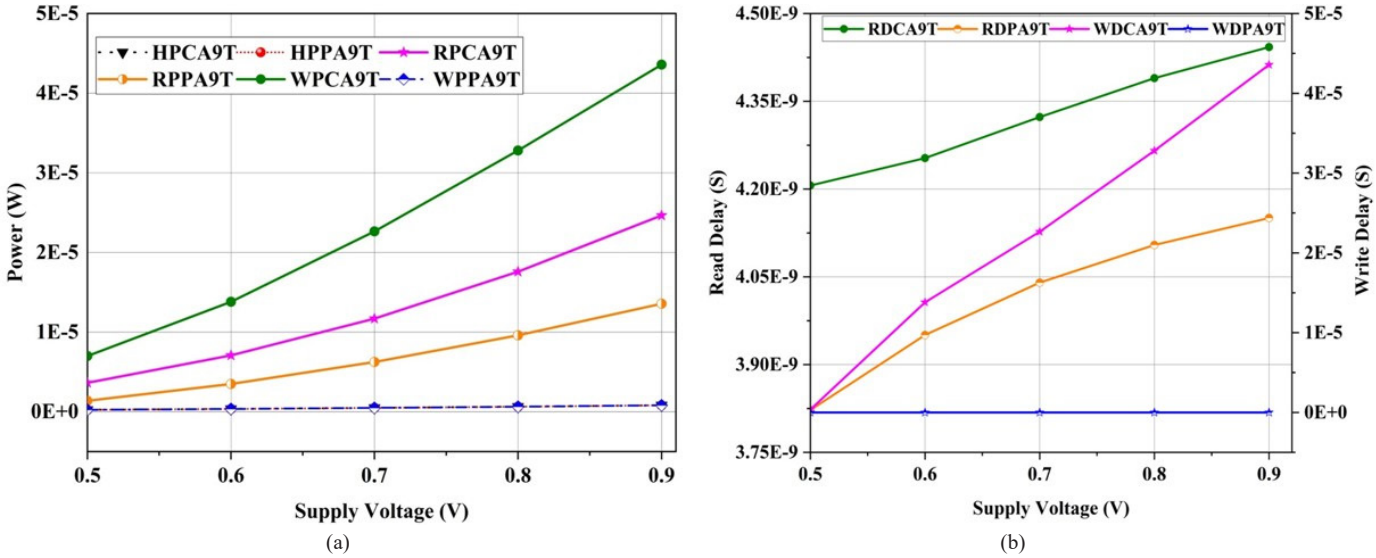
where W_G - total gate width, W_{min} - minimum gate width, N - number of CNT tubes and S - pitch [7]. Relation between the number of CNT tubes used in CNTFET and its 'on' current is

$$I_{CNFET} = N.g_{CNT}(V_{DD} - V'_{SS} - V_{th}) \tag{14}$$

where N - number of CNT tubes per device, g_{CNT} - transconductance, and V_{SS}' - voltage drop between the external and inner source node [7]. Equation (14) states that increasing the CNT tubes number, improves the 'on' current and the power consumption rises as given in Fig. 7 and delay is lowered.

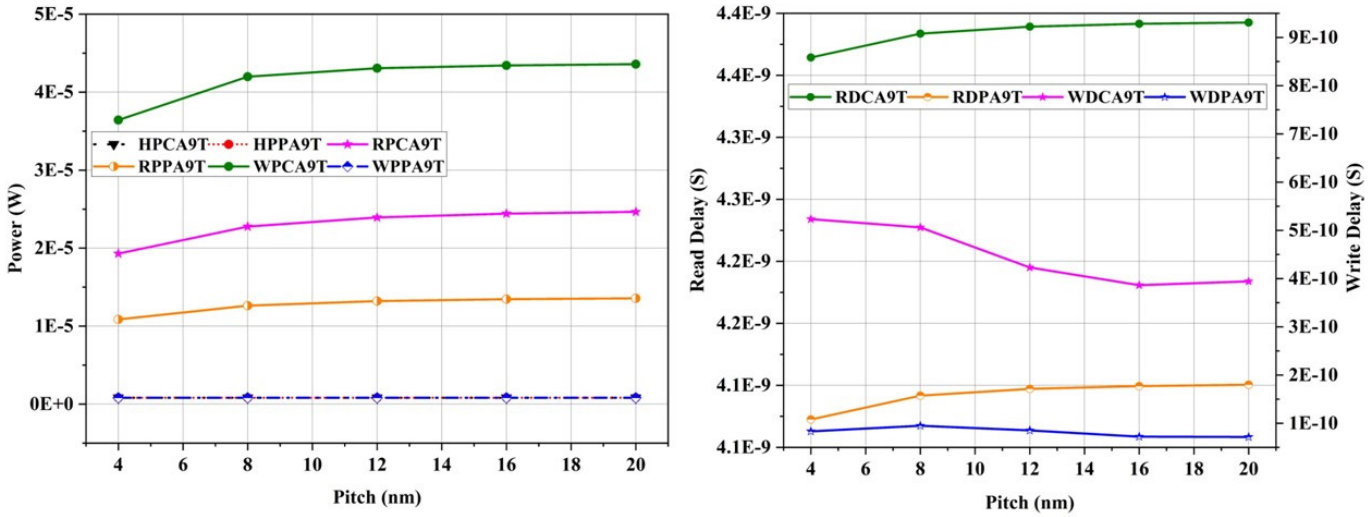
Dielectric material films are grown on top of gate of CNTFET. Power and delay for various dielectric materials like silicon dioxide (SiO2) with dielectric constant 4, Hafnium dioxide (HfO2) with dielectric constant 16, Zirconium dioxide (ZrO2) with dielectric constant 25, Tantalum pentoxide (Ta2O5) with dielectric constant 50 and Titanium dioxide (TiO2) with dielectric constant 80 is observed and the results are provided in Fig. 8. The current increases with dielectric constant resulting in higher power consumption and reduction in delay.

The results shown in Figs. 5 to 8 are averaged and tabulated in Table I and Table II. Percentage power reduction of PA9T with respect to CA9T is also given. Clearly, the performance of the proposed asymmetrical PA9T SRAM is better, under all parameter variations in view of circuit power and speed, especially in write power and write delay reduction, PA9T SRAM has high efficiency.



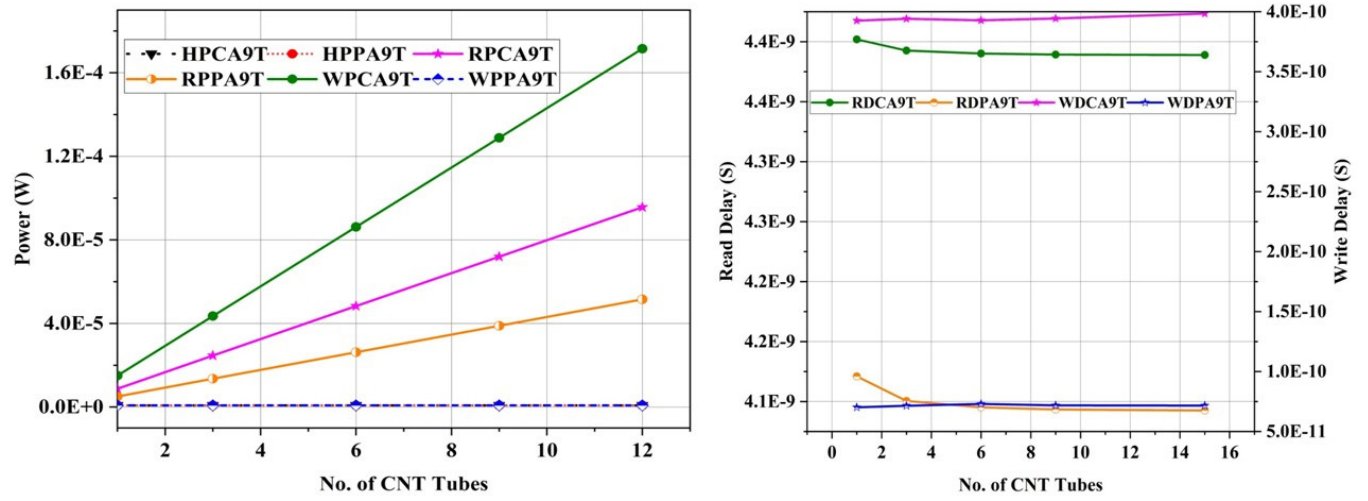
(a) (b)

Fig. 5. Voltage variations effect on (a) Power (b) Delay



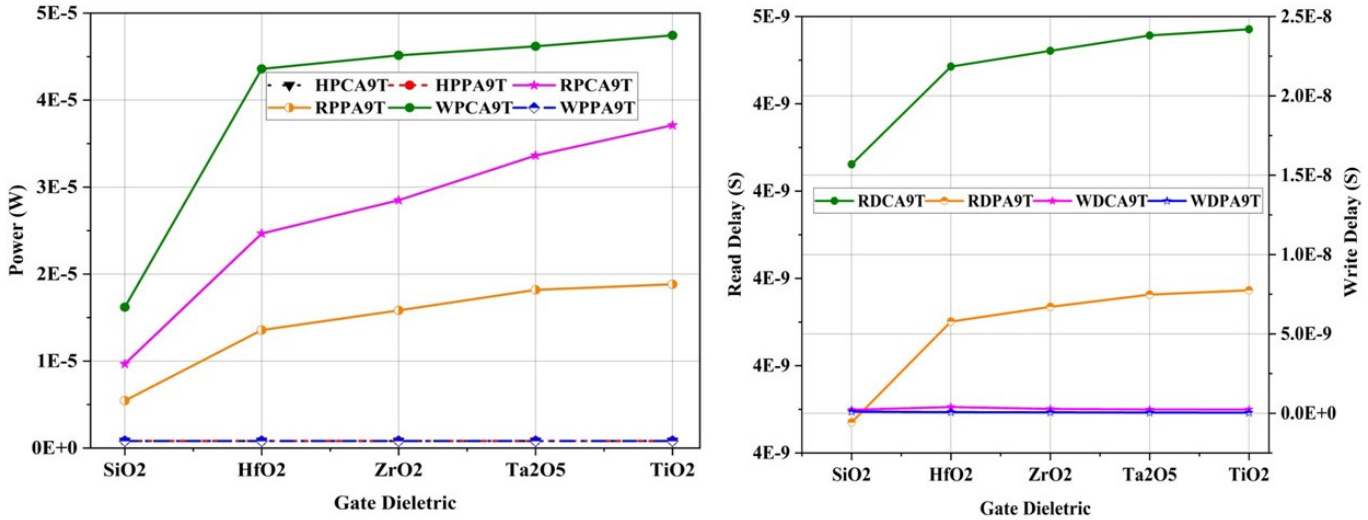
(a) (b)

Fig. 6. Pitch variations effect on (a) Power (b) Delay



(a) (b)

Fig. 7. CNT tubes variations effect on (a) Power (b) Delay



(a) (b)

Fig. 8. Gate dielectric variations effect on (a) Power (b) Delay

TABLE I
PARAMETER VARIATIONS EFFECT ON POWER

Parameters	CA9T SRAM	PA9T SRAM	%Power Reduction of PA9T
Effect of Voltage			
Hold Mode Power (W)	5.1047E-07	5.0999E-07	0.09
Read Mode Power (W)	1.2932E-05	6.8537E-06	47.00
Write Mode Power (W)	2.3969E-05	5.0999E-07	97.87
Effect of Pitch			
Hold Mode Power (W)	8.1171E-07	8.0998E-07	0.21
Read Mode Power (W)	2.3014E-05	1.2743E-05	44.63
Write Mode Power (W)	4.1698E-05	8.0999E-07	98.06
Effect of Number of CNT tubes			
Hold Mode Power (W)	8.1387E-07	8.0999E-07	0.48
Read Mode Power (W)	4.9874E-05	2.7070E-05	45.72
Write Mode Power (W)	8.9064E-05	8.0999E-07	99.09
Effect of Gate Dielectric			
Hold Mode Power (W)	8.1171E-07	8.0998E-07	0.21
Read Mode Power (W)	2.6712E-05	1.4372E-05	46.20
Write Mode Power (W)	3.9710E-05	8.0999E-07	97.96

TABLE II
PARAMETER VARIATIONS EFFECT ON DELAY

Parameters	CA9T SRAM	PA9T SRAM	%Speed Improvement of PA9T
Effect of Voltage			
Read Delay (S)	4.3228E-09	4.0136E-09	7.15
Write Delay (S)	2.2640E-05	9.1776E-11	100.00
Effect of Pitch			
Read Delay (S)	4.4343E-09	4.1423E-09	6.59
Write Delay (S)	5.2254E-10	8.1359E-11	84.43
Effect of Number of CNT tubes			
Read Delay (S)	4.4426E-09	4.1505E-09	6.57
Write Delay (S)	3.9447E-10	7.1605E-11	81.85
Effect of Gate Dielectric			
Read Delay (S)	4.4395E-09	4.1442E-09	6.65
Write Delay (S)	4.5591E-09	6.3931E-11	98.60

TABLE III
PARAMETER VARIATIONS EFFECT ON ENERGY

Parameters	CA9T SRAM	PA9T SRAM	%Energy Reduction of PA9T
Effect of Voltage			
Hold PDP (J)	1.4509E-11	4.4682E-17	100.00
Read PDP (J)	4.0313E-10	5.8230E-16	100.00
Write PDP (J)	7.3642E-10	4.4683E-17	100.00
Effect of Pitch			
Hold PDP (J)	4.2415E-16	6.5899E-17	84.46
Read PDP (J)	1.1644E-14	1.0332E-15	91.13
Write PDP (J)	2.1264E-14	6.5900E-17	99.69
Effect of Number of CNT tubes			
Hold PDP (J)	3.2105E-16	5.7999E-17	81.93
Read PDP (J)	1.9728E-14	1.9458E-15	90.14
Write PDP (J)	3.5231E-14	5.7999E-17	99.84
Effect of Gate Dielectric			
Hold PDP (J)	3.7007E-15	5.1783E-17	98.6
Read PDP (J)	4.8752E-14	8.0052E-16	98.4
Write PDP (J)	8.0502E-14	5.1783E-17	99.9

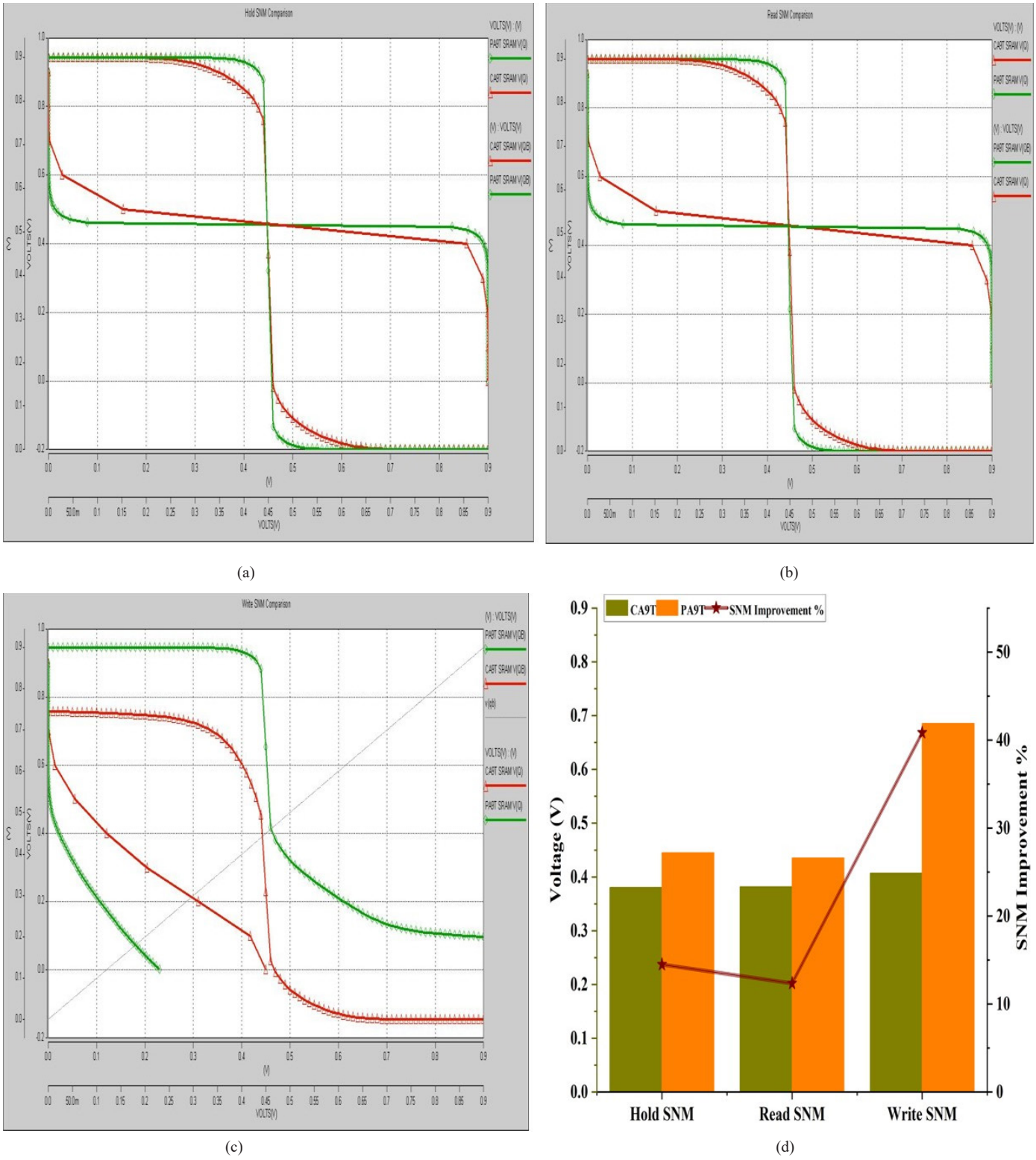


Fig. 9. SNM Comparison (a) Hold SNM (b) Read SNM (c) Write SNM (d) Percentage SNM Improvement

The most important concern apart from power and delay while designing a SRAM cell is its stability. Higher the stability or static noise margin (SNM) better is the memory cell's reliability and robustness. Stability of cell is estimated from the voltage transfer characteristics (VTC) of the cross coupled inverters in SRAM cell or from butterfly diagram. Butterfly diagram can be attained by merging the VTC of the cross coupled inverters by maintaining the SRAM in hold, read and write states. From the butterfly diagram, static noise margin (SNM) is measured by inscribing a square in the lobe and estimating its diagonal length. Fig. 9(a), Fig. 9(b) and Fig. 9(c) provides the butterfly diagram of CA9T SRAM and PA9T SRAM. On com-

paring the conventional and proposed SRAM it is found that the proposed PA9T SRAM hold and read stability is improved by 14% and 12% respectively. The write stability is highly enhanced in PA9T SRAM to about 41% than CA9T SRAM. The improvement in stability is due to the usage of HVT transistors and absence of P-type CNTFET in the proposed structure. Details about SNM values and percentage stability improvement are presented in Fig. 9(d).

Power delay product (PDP) is another important metric used to analyze the performance of VLSI circuits. PDP is the product of power and delay, and it implies the energy consumption of the circuit. Table III details the energy consumed by CA9T SRAM and PA9T SRAM due to parameter variations. PDP is evaluated for the same parameter values used to estimate power and delay, and all the corresponding values are averaged and given in Table III. It is obvious that the PA9T SRAM is better than CA9T SRAM with respect to energy also, and the energy reduction of PA9T SRAM varies from 82% to 100%.

IV. Conclusion

A CNTFET based SRAM which offers low power, low energy, high speed and enhanced stability is presented in this work. Supply voltage, pitch, number of CNT tubes and gate dielectric material are the parameters considered for the investigation. The performance of the proposed PA9T SRAM is better than the conventional CA9T SRAM proving it as a variations tolerant SRAM. Particularly PA9T SRAM read power, write power, write delay and PDP reduction is increased by 47%, 99%, 100% and 100% respectively. Write stability of the proposed SRAM is improved by 41% ensuring PA9T SRAM as a suitable structure for battery powered wearable devices in healthcare field where low power, high speed and reliability are of important concern.

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