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Editor's Column

Mladen Knezic

> Life is an eternal struggle. Who dares he can, who knows no fear goes forward.
>
> *Fieldmarshal Živojin Mišić*

Editorial Letter
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WE are pleased to begin this year with four compelling new papers and an exciting milestone: for the first time, "Electronics" has been ranked as a Q2 journal by SCImago, achieving an SJR score of 0.4999 in 2024. Additionally, Scopus has ranked the journal in Q3 with a CiteScore of 1.6 (34th percentile) for 2024.

These achievements reflect our ongoing commitment to enhancing the journal's quality through rigorous publishing standards and adherence to best practices. We extend our gratitude to our authors, reviewers, and readers for their invaluable contributions to this progress.

Looking ahead, we remain dedicated to further elevating impact and reputation of the journal. We invite researchers to submit their high-quality work and join us in advancing cutting-edge developments in different domains of electronics.

In the first paper, entitled "Intelligent IoT Surveillance and Instantaneous Management," Huang et al. proposed a fog-cloud-edge architecture enhanced with ResNetDL, a deep learning framework for industrial IoT. The system's efficiency is evaluated using experimental results in which the system ensures 35 ms latency, 58 fps throughput, 210 mJ energy, 55% resource utilization, and 42 ms response time compared to other methods.

The paper entitled "Wide-Band MIMO Antenna for Wireless Applications," authored by Chouhan et al., brings a design of a compact four-port wide-band MIMO antenna. Operating at 2.16–4.3 GHz, the antenna achieves high isolation (more than 12 dB), low Envelop Correlation Coefficient (ECC) (less than 0.03), and minimal Specific Absorption Rate (SAR) (8.83 nW/kg near the human head for 1g), making it ideal for 5G and IoT devices. The octagonal geometry balances performance and manufacturability.

In the third paper, entitled "Hardware Acceleration of Singular Spectral Analysis," Varma et al. implement an FPGA-based Singular Spectral Analysis (SSA) accelerator for Nuclear Quadrupole Resonance (NQR) signal denoising. Their HLS-driven design achieves a 15.48x speedup over ARM Cortex-A9, with 32.4 dB Signal to Noise Ration (SNR) improvement.

The last paper, entitled "CMOS Circuits Enhanced with Fe-MgO Tunnel Junctions," by Chakraverty and Ramakrishnan, reports the influence of magnetic tunnel junctions on the electrical response of an operational amplifier (op-amp). The simulation results prove that the introduction of tunnel junction increases the bandwidth and the phase margin of the circuit. Furthermore, the open loop gain also improves with the addition of tunnel junction as compared to the baseline op-amp simulation.

These contributions reflect the journal's commitment to bridging theory and practical innovation. Finally, I would like to extend gratitude to the authors and reviewers for their rigorous work and insights.

Intelligent IoT Surveillance and Instantaneous Management

Ying Huang, Yongmei Su and Shuanggui Lu

***Abstract*—Unmanned Vehicles (UVs) and the Industry Internet of Things (IoT) are two examples of new technology being incorporated into manufacturing processes during the fourth industrial revolution. IT networks must be machine-compatible to integrate these technologies; this includes addressing problems with connectivity, fog, and cloud-based computing security, lowering latency, and improving data reliability and standard of service. Regarding IoT, AI techniques must handle resource management, network deployment, and these problems. The significant issues are unstable and high-latency communications between Industrial IoT endpoints and the Cloud. By extending storage and computation to the network's edge, fog computing offers a valuable tool for merging intricately linked processing systems. Interoperability may be addressed using fog in an IoT gateway and advanced software distributed on the edge. However, as an IoT gateway is essential to processing and delivering data to many systems and platforms, selecting one is critical regarding accuracy and latency. Intelligent IoT monitoring and real-time control based on Integrating Autonomous Robots for Instantaneous Industrial Operations, visual recognition, and cloud/edge computing services are proposed to address these challenges. By deploying Deep Learning (DL) facilities close to customers who want them, latency and processing costs associated with transmitting data through the Cloud may be minimized. The suggested methods enhance platform decision-making and industrial automation system performance by integrating cloud-based services into an operational loop. A smart approach that offers a trade-off between accuracy and latency is suggested to choose the right AI for the situation under observation.**

***Index Terms*—Cloud computing, Edge computing services, Integrating autonomous robots, Visual recognition,**

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I. Introduction

MANUFACTURING has entered a new digital era, introduced by the Fourth Industrial Revolution [1], characterized by lightning-fast technical development. Uncrewed vehicles (UVs), automation through robots and AI, and the Internet of Things (IoT) [2], which connect physical things over the Internet, are vital technologies accelerating this change. Manufacturing IT networks must adapt to accommodate machines that use these technologies entirely. It includes fixing essential issues [3] with connection, security, latency, dependability, and quality of service. The unreliable, high-latency [4] interactions between industrial IoT endpoints and cloud computing services have been recognized as a severe obstacle. It makes real-time control, monitoring, and decision-making more difficult. Fog computing [5], which extends storage and processing capabilities to the network's edge, has emerged as a viable solution. It allows time-critical interactions between equipment, robots, sensors, and other endpoints [6]. Fog resources in IoT gateways can also address interoperability issues in industrial systems, software, and platforms. However, selecting the correct IoT gateway is critical since it organizes vital operations such as raw data processing and delivering valuable insights to numerous platforms [7]. Many researchers suggest implementing an intelligent system that utilizes fog computing, enhanced edge software, and strategic integration with cloud-based artificial intelligence to enhance factory automation [8]. A critical advancement is implementing deep learning capabilities at the edge, close to the source of data generation. This minimizes the delay and expenses of transferring substantial data to the Cloud [9]. Local execution enables the performance of crucial tasks such as visual identification, proactive maintenance, and immediate control of robots. The Cloud offers additional storage and computational capabilities to obtain long-term insights. This hybrid edge-cloud architecture enables the customization of the optimal combination of edge devices and cloud services [10] for individual functions. The edge handles jobs that need low latency, whereas the cloud architecture facilitates the ongoing improvement of complicated learning algorithms over extended periods. The system automatically distributes workloads across layers in response to the current condition and application needs.

Due to their high computation, administration, and storage needs, traditional techniques are no longer accessible on end devices. Because of this, to achieve the recently built edge-cloud monitoring with smart IoT applications, it is essential to use the lightweight learning model for intelligent object iden-

tification and to deploy the efficient training process in edge devices. Cloud monitoring systems have recently been popular among innovative applications because they emphasize managing the constantly generated data sequences from a comprehensive surveillance environment. Therefore, multi-object detection has gained a lot of interest from academics and businesses alike and has become a significant technology. Suppose innovative surveillance systems manage massive amounts of IoT data effectively. In that case, they must overcome obstacles such as the detection and localization of moving objects and the recognition and extraction of immediate features. This calls for powerful real-time processing capabilities. The proliferation of surveillance equipment and the ongoing improvement of large-scale, excellent surveillance data in IoT contexts pose increasing challenges to existing paradigms that rely on centralized processing. A primary issue is the widening disparity between the rate of data generation for surveillance and the capability of cloud-based data processing. The projected data captured by the camera alone will surpass 869PB by 2020's conclusion. In addition, new methods are needed to accomplish real-time, low-latency, energy-efficient, and highly accurate surveillance operations because of the enormous bandwidth requirements of transmitting massive volumes of data across Cloud surveillance systems. Creating a new edge-cloud monitoring architecture that moves the heavy processing loads away from the leading cloud server is crucial. Deploying the learned AI models in edge servers allows for the construction of an intelligent IoT system that efficiently addresses the aforementioned time-consuming issues through distributed and dependable computing.

State-of-the-art methods have shown promising results for identifying objects in static, stationary situations; nevertheless, handling complicated dynamic scenes remains challenging. Location, density, motion, and variations in illumination are some of the many variables that might impact object detection and tracking tasks in dynamic situations. Furthermore, present-day intelligent applications in ever-changing surveillance settings necessitate real-time data processing, communications, and control, including visual object detection, emotion analysis, and identity recognition.

UVs and autonomous robots equipped with sophisticated sensors are essential to their execution on the manufacturing floor. Edge computing [11] with computer vision and deep learning models allows the robots to react quickly to events as they happen. Under the guidance of a 5G connection, UVs oversee materials handling and inventory. Internet of Things [12] gateways clean, normalize, and route data flows from these devices to production dashboards, maintenance logs, and inventory management applications [13]. Cloud services offer centrally stored data lakes that may be used to aggregate datasets, find trends, and train prediction algorithms. These are subsequently distributed to edge devices for quick inference and automation. The hybrid design generates a responsive, intelligent system that supplements human operators. Because of edge, Cloud, and AI integration, manufacturing processes may be adjusted in real time while continually improving. This research offers significant insights into effectively utilizing fog computing, sophisticated edge software, and strategic coordination with the Cloud and AI to exploit the promise of new technologies in smart manufacturing fully. The suggested intelligent system attempts to augment automation, efficiency, quality, and production. The wide-ranging relevance in several industries, including automotive, pharmaceuticals, electronics, and others adopting the Industry 4.0 approach [14],

The objective and contribution of this research are listed below.

- To design the intelligent system architecture with the help of edge software, fog computing, Cloud, and AI integration to monitor optimized intelligent manufacturing applications.
- To apply deep learning techniques for addressing security, connectivity, reliability, latency, and quality of service challenges in information technologies.
- To provide edge-based solutions using deep learning capabilities to minimize the latency and cost of industrial IoT endpoints.

The rest of the manuscript is organized as follows: Section II describes the various researcher's opinions regarding the Industrial IoT endpoints related to intelligent solutions for the industry's multiple problems. Section III explains the working process of intelligent system architecture using edge computing and cloud applications. Section IV discusses the system's efficiency, and a conclusion is described in Section V.

II. Related Works

Essien and Giannetti introduced convolutional long short-term memory (CLSTM) in intelligent manufacturing to improve the system performance [15]. This study intends to improve throughput and reduce energy consumption. During the analysis, temporal and spatial distribution data is utilized on the CLSTM system to improve forecasting accuracy. The architecture has an encoder-decoder structure that explores every piece of information and maximizes industrial performance. The efficiency of the plant is evaluated in the United Kingdom, and the system ensures optimized results compared to other methods.

Chen et al. applied Deep Reinforcement Learning (DRL) in the industrial Internet of Things to manage the resources in mobile edge computing [16]. This work aims to minimize the delay and solve the Markov decision process problem. The introduced resource management process determines the policy gradient for every action and state. According to the actions, the resources are managed with minimum delay and maximum throughput.

Kishor et al. introduced the Intelligent Multimedia Data Segregation (IMDS) fog computing approach to minimize the latency in healthcare applications [17]. The IMDS approach uses the K-fold random forest approach to reduce storage, network, and transmission delays. The machine learning approach segregates the input using the random forest approach, which makes the healthcare decision up to 92% compared to other methods and reduces the latency by 95% compared to pre-existing models.

Fantacci and Picano recommended a constrained data offloading scheme (DCDO) for analyzing the performance of cloud-fog-edge systems [18]. This study uses the queuing theory to explore the performance of computing infrastructure. The requests are processed according to the deadline expiration using the Markov queueing system. In addition, the computation resource allocation approach is applied to maximize the quality of services in computing infrastructure.

Abbasi et al. applied a Genetic Algorithm (GA) with Intelligent workload allocation in Cloud and fog computing structure to maximize the allocation efficiency [19]. The ultimate goal of this study is to reduce delay and consumption power using the optimized resource allocation method. The green energy concept is initially applied to the multi-sensorial framework to manage data security. In addition, the GA approach is introduced to handle the large request volume by minimizing edge devices' delay and consumption power.

Mubarakali et al. suggested a delay-sensitive data transmission (DSDT) approach to managing multimedia applications' data storage and forwarding process [20]. The DSDT approach aims to create a robust solution while transferring data in fog computing with minimum delay. The approach processes the data nearer to the optimal network, and the solutions are selected by minimizing the latency. The practical exploration of sensitive data reduces the round trip time (15.67ms) and minimum delay on 1MB, 100KB, and 10KB data transmission.

Singh and Singh recommended the Energy Efficient Delay aware Task offloading (EEDTO) approach to manage the data in fog and cloud computing [21]. This study framework reduces the end-to-end delay according to the task allocation time. The optimal solution is framed by considering the edge server, IoT devices, and cloud components according to the delay. The offloading scheme is optimized using the levy flight moth flame optimization technique that reduces the energy by 22% compared to other offloading algorithms.

Siasi et al. introduced delay aware service function chain (DASFC) in hybrid fog-cloud computing to improve the computing performance [22]. The system aims to minimize the delay and manage the resources using the DASFC architecture. The system comprises a single cloud and fog layer that can handle the delay-tolerant and delay-sensitive information. The trade-off between the fog solution and Cloud standalone for every user request is examined to enhance the hybrid architecture. The effective utilization of this architecture minimizes energy consumption (28-30% less), realization cost (28-30% less), network delay (21-43% less), and high transmission ate (15-40% higher) effective.

Shukla et al. conducted a literature study to analyze latency in IoT using cloud computing techniques [23]. The study uses the PRISMA techniques to explore the various researcher's studies to minimize the latency for time-sensitive applications. During the analysis, 32 technologies and 23 approaches were analyzed via 112 papers, in which multiple researchers introduced IoT and AI techniques to minimize latency and improve throughput.

Jafari and Rezvani applied a non-dominant sorting genetic algorithm (NSGA-II) to optimize energy consumption and delay in IoT-fog-cloud computing [24]. This work aims to reduce the NP-hard and knapsack problems while solving the multi-objective problem. The sorting genetic algorithm is incorporated with the bee algorithm, providing optimal solutions with minimax differential evolution. The NSGA-II method examines every user request and provides the solution with minimum time delay, energy consumption, and high throughput.

Kuthadi et al. created a portable data security energy efficient framework (PDST-EEF) for managing data security in sensor networks [25]. This study uses the cryptographic signature model to identify different attacks. During the analysis, replay, and denial of services, attacks are identified while transferring data from the innovative grid environment. The framework observes every node's energy consumption; this factor maintains the network's reliability and throughput. According to various researchers' analyses, industrial applications' throughput, delay, energy, and other factors are maintained using artificial intelligence techniques. In addition, Cloud computing techniques and computing resources are widely applied to improve network performance. However, industrial operational resources fail to manage network reliability, connectivity, security, and latency, which are challenging.

The management of network dependability, latency, and security, together with the effective allocation of resources and the making of decisions in real-time, provide substantial challenges to industrial IoT systems. Certain parameters, such as energy consumption, delay reduction, and throughput, have been improved by existing technologies that use AI-based frameworks, genetic algorithms, and edge-cloud computing. However, these solutions often face challenges regarding scalability, flexibility to changing contexts, and the smooth integration of resource management and monitoring duties. Furthermore, when dealing with large amounts of data from diverse Internet of Things devices, most frameworks fail to perform strongly under real-time limitations. This paper proposes a deep learning framework called ResNetDL to overcome these constraints. It combines the characteristics of ResNet topologies with edge-cloud computing. Through the integration of residual learning, distributed IoT monitoring, and instantaneous resource management, ResNetDL presents a new method. By lowering latency, increasing task prioritization, and guaranteeing safe data transfer over the network, the framework is aimed to boost real-time performance. The suggested approach establishes a new standard in industrial IoT applications by optimizing energy efficiency, improving network stability, and facilitating smooth scaling by exploiting ResNet's excellent feature extraction capabilities and temporal-spatial data processing.

III. Analysis of Intelligent Iot Surveillance and Instantaneous Management using Cloud and Edge Computing Resources

The fourth industrial technology utilizes the Internet of Things (IoT) and Unmanned Vehicles to improve industrial performance. Information technology widely utilizes cloud computing technologies to address latency, computing security,

quality of services, and data reliability issues. Artificial Intelligence (AI) and Internet of Things (IoT) techniques are incorporated in industrial applications to manage the resources and network deployment that address the high-latency communication and unstable issues between the Cloud and industrial IoT endpoint. In addition, complex interconnected systems are developed using fog computing because it extends the storage and network computations, effectively resolving the interoperability issues. Therefore, the effective selection of an IoT gateway and real-time monitoring system is one of the crucial factors in improving the industry's performance. Hence, the main objective of this study is to enhance industrial automation and decision-making by integrating them with cloud-related operational loops. Then, the deep learning model is deployed in computing technologies to minimize costs and latency while transferring data to the Cloud.

There will be strong ties between current and future military actions and the organizational theology viewpoint on the effects and consequences that fully autonomous self-governing systems will have on humanity. The military is now creating and using technology with the express purpose of killing people. Numerous sectors can benefit from the combination of self-governing robots with IoT surveillance. Drones and robots that can navigate themselves can monitor vast regions, sending out notifications and live video feeds if something unexpected happens. Large buildings, like public areas, industrial sites, and warehouses, can benefit from this security. Preventing breaches and unauthorized access to data gathered by IoT devices and sent via networks requires strong security measures. Because there are so many different protocols and standards, it can be difficult for various Internet of Things (IoT) devices and robots to connect and collaborate without a hitch. Following rules concerning privacy, security, and the operation of autonomous systems is critical.

A. Designing the Intelligent System Architecture with the Help of Edge Software, Fog Computing, Cloud, and AI Integration

The main objective of this phase is to improve the smart manufacturing application's environment by creating an Intelligent System Architecture using fog computing, edge software, AI integration, and cloud computing. The framework utilizes the deep learning model on IoT gateway and fog nodes to minimize the latency while processing the network edges. The deep learning embedded edge nodes observe and visualize the real-time environment, and anomalies are detected effectively. Offload non-critical background activities to the Cloud strategically, such as data aggregation and model retraining. Create protocols for dynamic workload allocation at the edge and in the Cloud. Create cloud-based digital twin simulations that replicate physical processes and evaluate control rules. Then, the Intelligent System architecture is shown in Fig. 1.

Fig. 1. illustrates the design of intelligent system architecture for industrial applications. The structure consists of three layers: edge, fog, and Cloud. Each layer is optimized using deep learning techniques to improve industrial operations' robustness, flexibility, and scalability. The first layer is the edge, which consists of robots, smart sensor devices, machines, the Internet of Things, etc., connected to the physical environment. The fog layer has data analytics, machine-to-machine communication units, and optimization and analysis units that help to explore the edge node-connected information. Finally, the cloud layer provides cloud storage and a data centre that can process industrial details effectively. In this architecture, every layer is optimized with a deep learning technique that helps to improve the overall real-time monitoring and analysis system. Initially, the nodes in the edge layer collect the raw data $x(t)$ at t time from an industrial process. The collected information is preprocessed using fog nodes by executing the Mfog module, which is defined using equation (1)

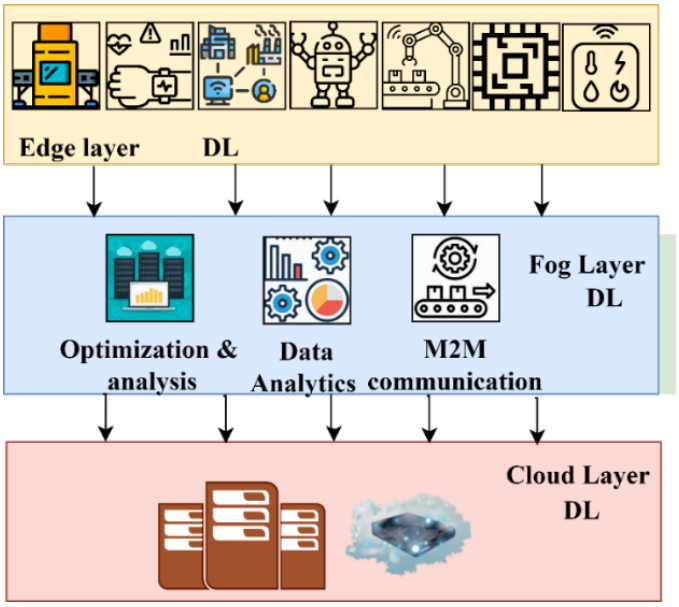


Fig. 1. Design of Intelligent System Architecture of industrial application

$$x'(t) = M\,fog\,(x(t)) \tag{1}$$

In equation (1), $x(t)$ is defined as collected raw data, Mfog is the fog module function, and preprocessed data is denoted as $x'(t)$. The fog layer facilitates adjacent computational capacity for edge devices, enabling real-time and low-latency artificial intelligence processing. To accomplish this, fog nodes such as gateways and servers would function as organizes for deep learning models tuned for efficient inference. Assume the fog node collects information using the IoT nodes from the industrial environment. The gathered information is processed using Convolution Neural Networks (CNN), identifying whether the device is defective. The convolution model is trained using ResNet architecture to explore the large data volume, which helps predict defective devices with minimum computation delay and error. The CNN network works according to the weight-sharing concept between the layers. Frequently updating weight factors minimizes the error rate and optimizes the network process. The ResNet architecture is shown in Fig. 2.

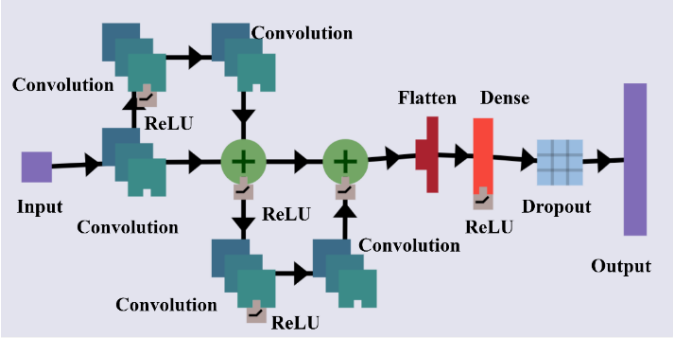


Fig. 2. Architecture of ResNet

Fig 2 illustrates the structure of ResNet, which includes several layers such as convolution, flatten, dense, and dropout layers. Each layer has a ReLU activation function to predict the output value. Here, the fog node collected input images are fed into the neural network that classifies the input as defective. The network has a sequence of convolution layers along with ReLu *(R(x))* that is defined as $R(x)= conv(ReLU(conv(x)))$. The *R(x)* is named as the residual block of the convolution layer. The residual block output is $R(x)+x$ in which x is defined as the identity pass-through. In the output computation, the neural network function is optimized using function *F(x)* and the residual block is described as $R^*(x)$. Then the $R^*(x)$ is estimated by subtracting *x* from $F(x)$; $R^*(x)=F(x)–x$. The network sharing weight between the layers and residual block parameters are utilized to train the network. The effective utilization of each parameter and function helps to reduce the vanishing gradient problems. The flattened layer in the network takes multiple inputs and produces a single output (defective or not). The sequence of convolution or other layers output is concatenated to obtain the output layer. The network output is optimized by incorporating the output layer that eliminates irrelevant information. For instance, when the rate is set to 0.1, the dropout layer will randomly choose 10% of the weights on each forward pass and put them to 0. Introducing a dropout layer with a rate of 0 will not impact the network; however, a rate of 1 will cause the dropout layer to produce an output of 0. The overfitting issue is eliminated with the help of a regularization process in which new terms are added to the solution. The input pairs $\{(x_1, y_1), (x_2, y_2),.....(x_n, y_n)\}$. The function *f* is utilized to predict the output for the given input by addressing the classification problems. The classification problem is defined as $min_f \sum^{n}_{(i=1)} C(f(x_i), y_i)$. Here, *C* is the cost of $f(x_i)$ prediction when the y_i true value. Then, the regularized loss value is defined as $min_f \sum^{n}_{(i=1)} C(f(x_i), y_i) \mid \lambda R(f)$. The regularization term $R(f)$ is larger when $\lambda > 0$ and larger f. Then, the regularization is performed using the L2-norm, which is defined as $\sqrt{(\sum_i \sum_j a^2_{ij})}$. During training, dropout layers selectively disregard a random portion of the input units. For further details, please refer to our explanation on dropout layers. There are two rationales for why dropout aids in mitigating overfitting. Dropout may be seen as a form of ensemble learning wherein weak classifiers (prone to underfitting) are combined by aggregating their classifications, such as selecting the majority class. Each batch involves training a new network portion as a weak classifier. The whole network is utilized during validation, essentially amalgamating all classifiers to yield a singular outcome. An alternative perspective suggests that via several iterations, dropout compels the utilization of all components within a network design. Consequently, the absence of one characteristic in the training set will prevent excessive influence, thereby preventing the network from fixating on exclusive anomalies. In industrial applications, fog nodes run the ResNet deep learning model on real-time analysis, which is defined as $y(t) = Zfog(x'(t))$; $y(t)$ is represented as the real-time control and automation output at the edge. Then, non-critical data is flattened and sent to the Cloud for periodic retraining. The retraining process is defined as $zcloud = retrain(aggregate\ (x'(t)))$. The refined models are gradually redeployed to the fog and edge devices to enhance processing capabilities over time. During the output estimation, load balancing between cloud and fog was controlled according to the edge computing load, available bandwidth, and expected cloud latency. It enables the optimization of task distribution by utilizing the capabilities of both edge and cloud computing.

B. *Applying deep learning techniques for addressing reliability, latency, security, and connectivity issues*

The main intention of this objective is to improve security, latency, reliability, and connectivity in industrial information technologies. Implement decentralized identification and access management by utilizing blockchain-based ledgers on edge nodes. Then, end-to-end encryption across the edge, fog, and cloud layers is applied to improve the system's security. In addition, deep learning models reduce the time delay and usage of resources for deployment on edge devices. The redundancy and fail-over measures enhance dependability by examining the patterns of network traffic and allocating resources to the edge and fog computing systems accordingly. The network uses the blockchain ledges on edge nodes for access and decentralized identity management. Blockchain technology enables decentralized identity and access management across the system architecture's edge, fog, and cloud layers. Every edge device, such as a sensor or robot, would own a distinct digital identity recorded on an unchangeable blockchain ledger. Intelligent contracts will incorporate access controls that dictate the devices authorized to access particular fog and cloud resources. The edge computing block ledger is represented as $blockchain\ ledger_{edge}=\{block_1, block_2, \ldots\ldots block_n\}$. Each block has transactions associated with forming identities, access requests, and ledger revisions. This architecture utilizes blockchain technology's decentralized and transparent characteristics to improve identity and access management, especially in edge computing contexts where dependability and rapid decision-making are essential. The permissions are subject to cryptographic signing and verification through the ledger. Edge devices require only their private key to authenticate and obtain authorization to access fog/cloud servers. This eradicates individual vulnerabilities such as credential storage. The distributed ledger enhances the system's resilience against disruptions. Access that has been revoked can also be spread throughout the whole system

through blockchain transactions. The decentralized method of managing identity and access ensures optimal security while maintaining scalability across edge-fog-cloud architecture. Gateways provide a smooth connection between modern and outdated systems, covering from the periphery to the Cloud. They achieve this by encapsulating and converting industrial protocols into IP packets. Middleware software facilitates the interaction between protocols using APIs, whereas adapters convert data formats. Interoperability is guaranteed by using protocol converters that connect different standards. Redundant multi-path routing ensures strong communication across the edge, fog, and cloud architecture. 5G wireless technology with high bandwidth and slicing ensures dependable and low-latency machine-to-machine communication. Network traffic engineering utilizes artificial intelligence algorithms to make forecasts, implement quality of service regulations, and use rate limitation techniques to optimize data flow depending on their priorities. These extensive communication mechanisms enable smooth and two-way data flow across various new and old applications, equipment, standards, and suppliers in contemporary industrial contexts. The integration allows for the complete utilization of developing technology. The connectivity is established at the edges by integrating the protocol converters and gateway devices. The edge connectivity is described in Fig. 3.

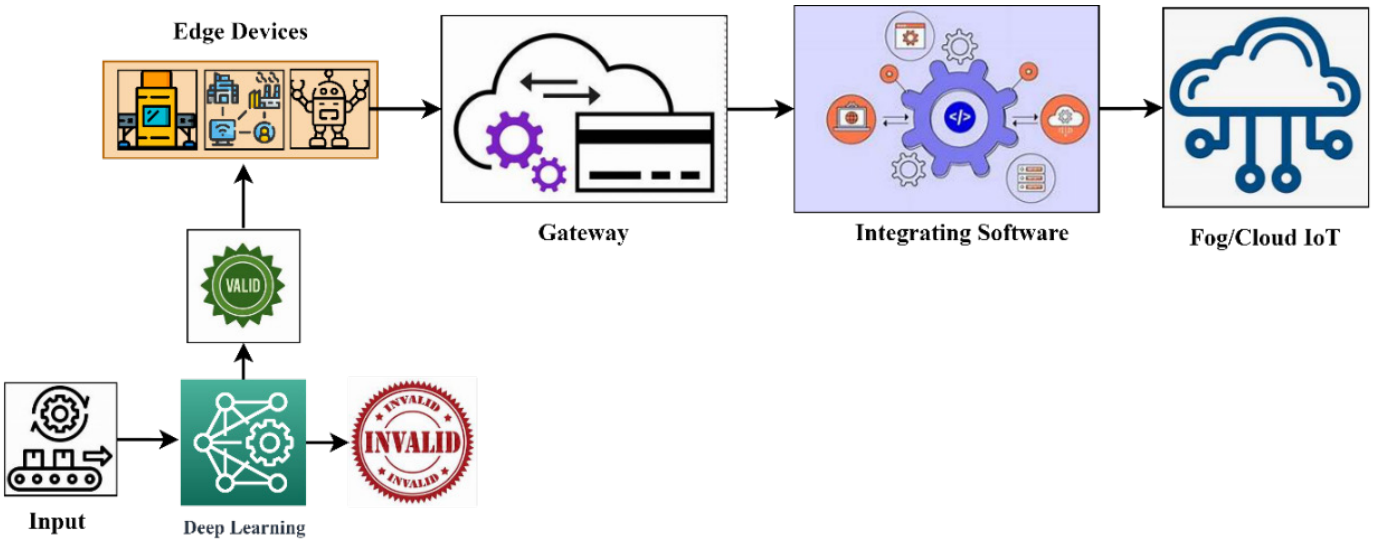


Fig. 3. Analysis of Edge Device Connectivity

The edge network uses the deep learning network ResNet to optimize the overall connections and data distribution. The ResNet uses the residual blocks and collection of layers to validate whether the devices are defective. The optimization model uses pruning that eliminates the non-critical parts in the inputs using layers, filters, and connections. The pruning process minimizes the parameters and computation complexity. During the output estimation, the network uses the lower bit precision (8-bit integer) to signify the weight values and the 32-bit floating point activation function that compresses the model size. This process is named quantization, which reduces the latency while processing the information in industrial applications. In addition, the knowledge distillation and ResNet model has depthwise convolutions that require minimum computation to process large volumes of data. The model minimum complexity process is described in the flow of *cloud model (Mcloud)→model optimization→edge model medge*. Here *size (medge)"size (Mcloud)* which allows the low-latency at edges *latency(medge)<latency(mcloud)*. Implement distributed authenticated access control using blockchain-based identity ledgers. Encrypt data from beginning to finish using hardware security modules installed on gateways. Use protocols like TLS, VPNs, and HTTPS to prevent man-in-the-middle attacks and ensure secure communications. Keep non-essential networks and operations at the periphery of the network disconnected. Complete reliability measures that cover the edge, fog, and cloud levels provide a robust architecture. The system may seamlessly switch to a backup computer or network in a breakdown. Regular backups and snapshots allow for quick recovery, and data is safeguarded by node replication. Anomaly detection and constant health monitoring help find system faults immediately so that preventative maintenance may be done. A buffer of capacity is set aside to handle unexpected surges in demand. The Cloud offers almost infinite burst capacity on demand if edge resources are exhausted. Proactive prevention, quick detection, and minimum disruptive recovery from equipment failures and outages guarantee the continuation of industrial activities through these multi-layered dependability solutions, which offer resilience across heterogeneous infrastructure. The different controls optimize operating and capital costs while providing defense-in-depth.

C. Arrange edge-based solutions to reduce cloud dependence.

Lightweight deep learning models are implemented directly on IoT gateways and bypass the Cloud to provide sophisticated analytics and real-time control at industrial IoT endpoints. The gateways utilize specific AI acceleration modules to execute

optimized neural network models for low-latency inference. For example, a gateway can examine camera input in real time to detect faults using a compressed convolutional neural network model. Similarly, deep learning networks use vibration sensor time series to predict when equipment will break. Avoiding the high latency, network costs, and connection demands of cloud-centric techniques is possible by keeping computation utilizing edge gateways. Cloud computing allows for infrequent model retraining using aggregated data instead of continuous real-time analytics. Therefore, intelligent edge-based solutions can realize the potential of AI and automation at the industrial edge while overcoming the limitations associated with cloud dependency. At the outermost edges of the network, industrial IoT endpoints such as sensors, equipment, and robots produce massive volumes of data.

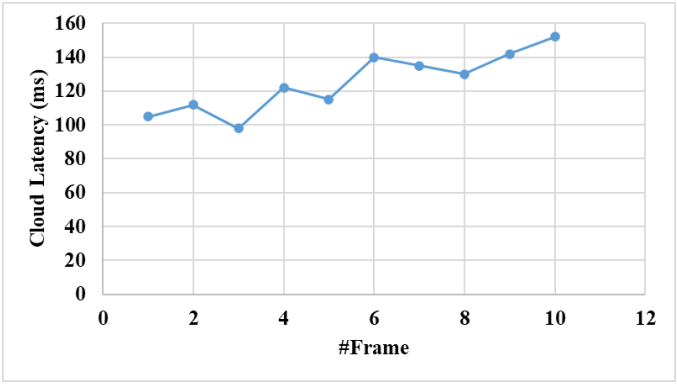
Nevertheless, there are significant concerns with dependability, bandwidth costs, and latency when transferring all this raw data to the Cloud for processing. Deploying on-premises AI-enabled IoT gateways enables real-time intelligent analytics and control at the edge, overcoming these issues. For low-latency deep neural network model execution, the gateways use model optimization approaches with purpose-built AI accelerator modules such as VPUs, TPUs, or FPGAs. For instance, by analyzing video feeds from cameras on production lines, computer vision models such as MobileNets and object detectors may detect errors or track inventory in real time. Through source-level modelling of temporal sensor data, deep networks can anticipate equipment breakdowns. Robots with deep reinforcement learning agents can learn to manipulate items more efficiently in different environments. Before being compressed and sent to the edge gateways, these optimized deep learning models undergo training on the Cloud utilizing rich aggregated datasets. Gateways receive data in real-time from local IoT endpoints, process it using AI models at sub-second timeframes, and then act or control without involving the Cloud again. It is possible to retrain the models worldwide by sending data from the gateways to the Cloud regularly, often daily. However, local processing takes care of the real-time details. This lessens the risks of centralized cloud deployment, such as bottlenecks, SPOFs, and attack surfaces. Intelligent gateways enable industrial IoT to secure the benefits of deep learning at scale and in real-time, unlocking the promise of edge automation and control driven by AI.

IV. Results and Discussions

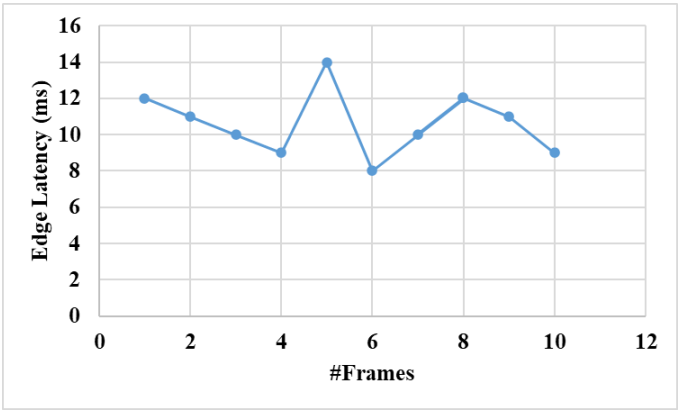
This section explores the excellence of Intelligent IoT Surveillance and Instantaneous Management using Cloud and edge computing resources using ResNetdeep learning techniques (ResNetDL). This study uses the Open-industrial-datasets (https://github.com/AndreaPi/Open-industrial-datasets) to analyze the performance of resource management and analysis. The dataset consists of several datasets, such as the Turbofan Engine Degradation Simulation Data Set, VSB Power Line Fault Detection Dataset, etc. This dataset information is collected and processed using deep learning-based fog-cloud and IoT computing technologies. The techniques recognize the defective information from the collected data used to process the user request with effective latency, throughput, energy consumption, resource utilization, and response time. The efficiency of the system is evaluated and compared with existing systems such as convolutional long short-term memory (CLSTM) [15], Deep Reinforcement Learning (DRL) [16], Intelligent Multimedia Data Segregation (IMDS) [17], and non-dominant sorting genetic algorithm (NSGA-II) [24].

A. Latency Analysis

Latency is the time delay between the input frame captured in the surveillance system and the decision made for the input. The mean processing duration for a frame as it travels from the edge to the Cloud and then returns are determined in the latency analysis. In addition, the latency is estimated by taking the ratio between the total processing time and number of frames. The latency value is analyzed for Cloud and edge; the results are illustrated in Fig. 4.



(a)



(b)

Fig. 4. Latency Analysis of ResNetDL: (a) Cloud and (b) Edge latency for number of frames.

The measurements indicate the cloud and edge inference delay on sample frames obtained from a video stream. The cloud latency varies between 98ms and 152ms due to network-related issues. On the other hand, the deep learning model that has been tuned and is being executed on the edge gateway achieves

significantly reduced latency, ranging from 8ms to 14ms per frame. This allows for immediate analysis of video data and prompt response at the edge, as opposed to a delayed reaction from the Cloud. Over some time, the accumulation of hundreds of milliseconds results in substantial latency for industrial control systems. Implementing deep learning algorithms at the edge enables rapid closure of control loops, resulting in enhanced automation and improved quality. Further excellence of the ResNetDL latency value is compared with existing methods, and the obtained results are shown in Fig. 5.

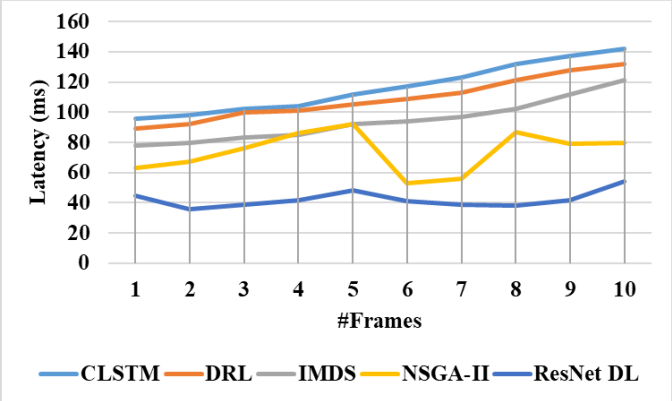


Fig. 5. Latency Analysis

The ResNetDL technique, which utilizes an improved ResNet model on the edge gateway, delivers a reduced latency of 42.4ms for real-time computer vision. This enables quicker defect detection and process management. These enhanced deep learning methods decrease latency in comparison to cloud-based processing. However, the compact ResNetDL model provides the quickest inference for time-sensitive industrial automation applications. The ResNetDL methodology achieves the lowest latency compared to other deep learning techniques because of its optimized model design, and deployment centred on edge devices and efficient process. The residual connections in ResNet enable the creation of precise models with greater depth while using fewer parameters. Complexity is further reduced by model optimization techniques such as pruning, quantization, and compact design. Eliminating network latency is achieved by executing the optimized model on specialized AI accelerators at the edge gateways close to the data source. Local processing is limited to core inference, whereas preprocessing and retraining are performed in the Cloud. Automated hyperparameter adjustment optimizes the model to achieve optimal performance on low-latency edge devices. Using quantized math, streamlined frameworks, and eliminating unnecessary repetition directs the emphasis of inference onto the fundamental calculations. By combining these methods, ResNetDL achieves extremely low latency in milliseconds while maintaining high accuracy. By being responsive, this capability enables the utilization of real-time artificial intelligence to optimize the worth of industrial data for intelligent management and automation.

B. Throughput Analysis

The throughput metric measures how effectively the ResNetDL process processes the video frames. During the analysis, the number of frames is assessed per unit of time, and the ratio between the number of frames and processing time is computed. The results are illustrated in Fig. 6.

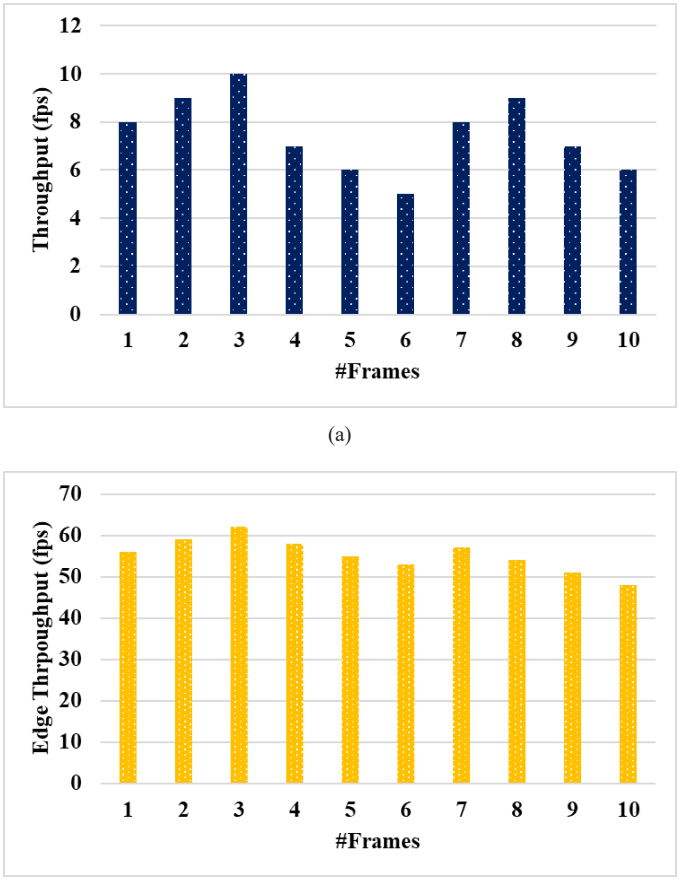


Fig. 6. Throughput Analysis of ResNetDL: (a) Throughput and (b) Edge Throughput for Number of Frames

The measurements indicate the frames per second (fps) throughput for cloud and edge inference on sample frames obtained from a video stream. The Cloud's data transfer rate varies between 5 frames per second (fps) and 10 fps because of constraints in network capacity. On the other hand, the enhanced deep learning model executed on the edge gateway locally produces much greater throughput, ranging from 48 frames per second to 62 frames per second each frame. The ResNetDL approach achieves efficient localized edge processing by improving the deep learning model, resulting in effective high throughput. Pruning and quantization reduce redundant processes and data transport, focusing computational resources on crucial activities. The ResNet architecture, designed to be streamlined, decreases model complexity compared to more extensive networks located in the Cloud. Performing inference on dedicated AI accelerator chips at the edge enables optimized hardware performance, circumventing constraints imposed by

network bandwidth. The edge can prioritize time-sensitive inference by transferring fewer essential operations, such as data collection and model retraining, to the Cloud. Automated optimization precisely tailors the model to maximize the throughput of edge devices. Optimizing the utilization of indigenous resources attains a throughput of more than 5-6 times greater than methods prioritizing cloud-based techniques. By executing advanced artificial intelligence algorithms directly at the origin, industrial systems can maximize the use of data and achieve effective real-time processing rates.

C. Energy Consumption Analysis

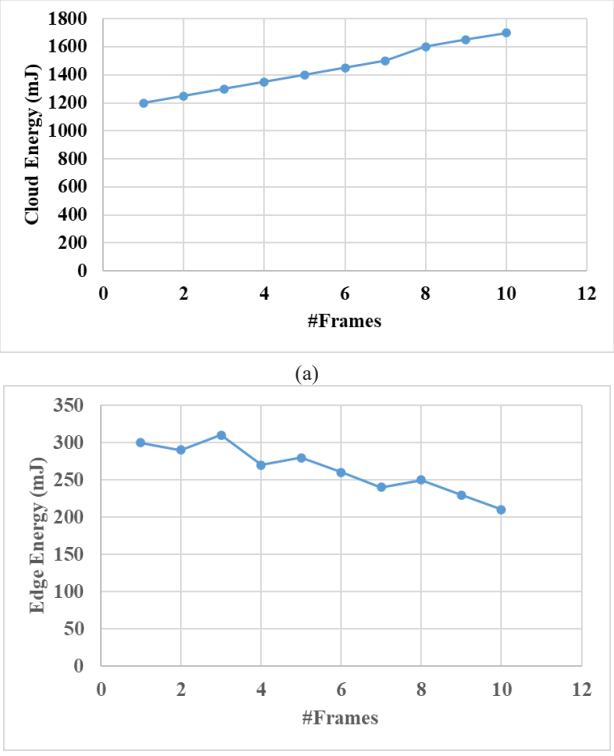


Fig. 7. Energy Consumption Analysis of ResNetDL: (a) Cloud Energy and Edge Energy for Number of Frames

Energy Consumption Analysis are illustrated in Fig. 7. The measurements indicate the energy usage, measured in milliJoules, for both cloud and edge inference per video frame. The cloud inference process uses an energy range of 1200-1700 mJ per frame, primarily attributed to the expenses associated with network transmission and data centre energy consumption. On the other hand, the highly efficient specialized hardware allows the optimized deep learning model to use just 210-310 mJ per frame when executed on the edge device. This leads to a more than 80% reduction in energy usage by performing processing at the edge instead of in the Cloud. Local edge analysis minimizes wasted energy on networking and uses efficient inferencing devices. ResNetDL reduces energy usage by utilizing efficient edge devices for local on-site processing rather than relying on energy-intensive cloud data centres. Using optimized model architecture and inferencing hardware decreases computational demands compared to resource-intensive cloud networks. The ResNet architecture, which is small, reduces energy consumption by utilizing residual connections and pruned layers to decrease computationally costly calculations. AI accelerator chips such as VPUs and TPUs are designed to optimize performance per watt for specific workloads. Through the analysis of data at its origin, there is no unnecessary energy expenditure in transporting the data to the Cloud and then receiving it back. The optimized framework prioritizes critical real-time inference at the edge, eliminating extra processes. Automated optimization adjusts the model hyperparameters to decrease computational requirements while retaining the accuracy criteria. In addition, the system's efficiency is evaluated and compared with existing systems, and the results obtained are shown in Table 1.

TABLE I
PERFORMANCE ANALYSIS

Metrics	Latency (ms)	Through-put (fps)	Energy (mJ)	Resource Utilization (%)	Response Time (ms)
CLSTM [15]	62	45	350	68	74
DRL [16]	71	41	410	72	82
IMDS [17]	53	49	310	65	63
NSGA-II [24]	82	37	460	78	94
ResNetDL	35	58	210	55	42

Table I demonstrates the superior performance of the proposed ResNetDL approach compared to existing deep learning techniques in essential system parameters crucial for industrial applications. ResNetDL achieves a latency of just 35ms by utilizing a simplified model architecture and deploying it directly on-site, minimizing any delays caused by network communication. By effectively exploiting local edge resources, it achieves a throughput of up to 58 frames per second, overcoming the limited performance of cloud-based systems. The energy usage is reduced to 210 millijoules per frame by immediately processing the data at its origin rather than transferring it to the Cloud. ResNetDL achieves a resource consumption of just 55% due to its efficient and compact model architecture. This corresponds to an impressive reaction time of 42 milliseconds, demonstrating exceptional real-time performance. CLSTM, DRL, IMDS, and NSGA-II demonstrate increased latency, decreased throughput, heightened energy usage, and slower reaction times due to their utilization of bigger and more intricate models and reliance on cloud services. ResNetDL enhances the performance of edge devices by tailoring the model to their requirements. This results in improved use of industrial data streams, reduced delay, increased data processing capacity, enhanced energy efficiency, and quicker AI responses at the real-time edge.

In comparison to other methods that aim to reduce delays in hybrid fog-cloud systems, our system achieves a much lower latency of 35ms, outperforming models like the delay-sensitive data transmission (DSDT) [20] and the delay-aware service function chain (DASFC) [22]. The suggested ResNetDL architecture substantially reduces latency, guaranteeing speedier real-time processing crucial for vital decision-making tasks and immediate IoT monitoring. Compared to methods such as

Intelligent Multimedia Data Segregation (IMDS) [17], which achieved 92% accuracy without prioritizing frame-rate processing speed, the system's throughput of 58 fps allows it to manage large data quantities efficiently. This innovation shows the capacity of ResNetDL in real-time applications that need high-speed data processing. Models such as the Energy Efficient Delay-aware Task Offloading (EEDTO) [21] lowered energy consumption by 22%, but the system's 210mJ utilization is much lower. ResNetDL guarantees long-term viability in power-constrained contexts by optimizing energy efficiency without sacrificing performance. Compared to methods such as the constrained data offloading scheme (DCDO) [18], which uses queuing models to control computational resources, the suggested framework achieves balanced resource usage at 55%. ResNetDL's optimization algorithms improve system scalability and resilience by preventing resource underutilization or overload. The framework's lightning-fast flexibility to user demands is on full display with a 42ms response time, surpassing solutions such as NSGA-II [24], which excels at delay-sensitive activities but struggles to achieve real-time systems' sub-50ms response time requirements.

V. Conclusion

Thus, the paper analyzes the ResNet Deep Learning (ResNetDL) approach-based industrial automation operation process using the IoT-fog-cloud computing technologies. The optimized deep learning model-based created intelligent system architecture reduces the latency while transmitting data in the cloud and fog computing technologies. The deep learning model uses pruning and weight optimization during the input classification. The frequent updating of network parameters successfully identifies defective and standard information. Then, the edge, fog, and cloud layers create an effective gateway to transmit the information. In addition, the edge layer uses the blockchain ledger that reduces security-related issues and effectively maintains reliability, scalability, and connectivity. The system's efficiency is evaluated using experimental results in which the system ensures 35ms latency, 58fps throughput, 210mJ energy, 55% resource utilization, and 42ms response time compared to other methods. In the future, meta-heuristics optimization algorithms and deep learning models will be utilized to improve the overall performance of data analysis in industrial applications.

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A cutting-edge Wide-Band MIMO Antenna for Modern Wireless Applications

Sanjay Chouhan, Debendra Kumar Panda, Sarthak Singhal, and Jitendra Yadav

***Abstract*—The present work explores the insights of a design which is defined as an octagonal geometry based four port wide-band MIMO antennas for wireless systems. The isolation essentialities have been considered through the parasitic elements (PE) with T-shaped isolation structure for isolation boost. The antenna under consideration is optimized to achieve the best MIMO performance parameters. It has functional band of 2.16-4.30 GHz and the antenna fabricated on substrate size of 60.0 X 76.0 mm^2. The gain 3.44 dBi, envelop correlation coefficient (ECC) < 0.03, and mean effective gain (MEG) ≤ -2.90 dB are achieved. The total active reflection coefficient (TARC) bandwidth is found 1.35 GHz. The specific absorption rate and channel capacity loss are evaluated, and both found to be within acceptable limit recommended by international telecommunication union (ITU). The results obtained through the proposed design are found to be within the acceptable limits of stability for effective communication system.**

***Index Terms*— Diversity, ECC, MIMO antenna, TARC Bandwidth.**

Original Research Paper
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I. Introduction

WIRELESS communication technologies are changing rapidly and need continuous intervention from the researcher's side. The growth of contemporary wireless applications, including 3G, 4G and 5G networks, Internet of Things (IoT) gadgets, and high-speed data transfer, has a need for extremely effective and adaptable antenna systems [1]. A radical expansion in wireless communication has been observed in recent years viz. continuous exploration in designing specific antennas capable of adapting various frequencies and providing dependable performance in a wide range of applications [2]. Maintaining great signal quality is a challenge for antennas designed to handle wider frequency bands [3]. Wide-Band MIMO antennas are a game-changing advancement in wireless communication technology, promising improved performance and adaptability in a variety of contemporary wireless applications [4]. These antennas can send and receive numerous data streams simultaneously thus greatly enhancing communication efficiency and data throughput [5].

The compact dimensions of these MIMO systems lead to higher coupling of elements, which results into degradation of system's overall performance. In the available literature [1]-[34], researchers have reported multiple ways to minimize mutual coupling or to enhance inter port isolation. Some of those techniques are split ring resonator (SRR), coupling networks, de-coupling isolating structures, PE, metamaterials, slot loaded radiator or ground plane, modified feed-line, modified ground plane, modified radiator, cross-coupled semi loop (CCSL), flag shaped stub, tunable network etc. All the above discussed geometries have either narrow bandwidth or large dimensions. Thus, various techniques used for isolation and capacity enhancement have been reported in literature in last decade. A few MIMO antennas design tried to enhance capacity and, isolation and identification of radio frequencies by leaky-wave radiator for 2.45-GHz [6]. In addition, DGS fulfilled the requirement of isolation up to some extend by disturbing or changing the direction of surface current [7]. The change in current direction fosters improved isolation by cancelling the inner element currents. The same attributes can also be achieved by polarization diversity [8]. Some of the applications require appropriate isolations for the optimum performance such as 2 x 2 MIMO antennas for USB application [9]. In compact antenna design isolation can be improved by hybrid balun circuit [10]. Apart from this the isolation achievement in dual band antenna for all bands has put challenges to the research community [11]. Sometimes the slotting in antenna has emerged out as one of the important techniques for isolation enhancement [12]. The isolation technique improves the isolation but it also shifts the resonating frequency [13]. Thus, the placement of isolating elements requires lot of analysis and precautions [14]-[15]. The CSRR structure is also instrumental in producing good isolation among antenna ports [16]. Optimum isolation in compact antenna is also one of the complex tasks in compact antennas [17]-[18]. Presently, some of the techniques [19]-[20] for MIMO antenna isolation enhancement have become obsolete and new techniques and tactics like metamaterial, hybrid ring, and resistive elements for single band and multiband applications are in developing phase [21]-[22]. Sometimes the shape of antenna also gives better results from isolation point of you, like use of some serpentine structure, some non-mathematical structure etc. [23]-[24]. The non-mathematical structure is generally generated by hit and trial method

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and on the basis of trail the performance of the antenna is observed [25]-[26]. Flag shaped stub, dual feeding, tunable network, fractal antenna and CE radiators had also been capable of in achieving good isolation among antenna elements [27]-[28].

Though a great deal of study has been done and is documented in the literature to attain optimal isolation, efforts are always being made to use novel approaches in order to obtain improved results [29]–[30]. The goal of the suggested study is to minimize port coupling and arrive at the ideal MIMO parameter value. Good isolation, higher efficiency, a wide bandwidth, and optimal gain are a few of the goals of the suggested work that are successfully met. To improve isolation, the current work uses a modified feeding strategy, PE, partial ground approaches, and a folded T-shaped structure.

The present work offers a Wide-Band Multiple-Input Multiple-Output (MIMO) antenna that is specifically engineered to satisfy the stringent requirements of modern wireless technologies. This study examines the design, creation, and characterization of a cutting-edge Wide-Band MIMO antenna that not only addresses these changing issues but also helps to improve the infrastructure for wireless communication. The complexity of this antenna's design, its amazing wide-band capabilities, and its potential to revolutionize contemporary wireless applications are all covered in the parts that follow. This study marks a significant advancement in the search for antennas that can keep up with the rapidly changing wireless communication environment.

Four uniformly shaped elements are used in this design for wideband 2.16–4.3 GHz applications.

The numerous MIMO antenna performance characteristics are examined and measured to provide the best possible performance of the MIMO antenna design. This study proposes an full octagonal shaped antenna for wireless applications using MIMO techniques. The reported antenna geometry offers several advantages, including a broader working bandwidth, minimal ECC, and compact dimensions. The antenna geometry is created, studied, and optimized using the CST MWS simulator and fabricated on FR4 substrate. The simulated results are verified by measured results. The design antenna uses two isolation methods for upgradation of isolation among antenna ports.

II. Antenna Design, Methodology And Material

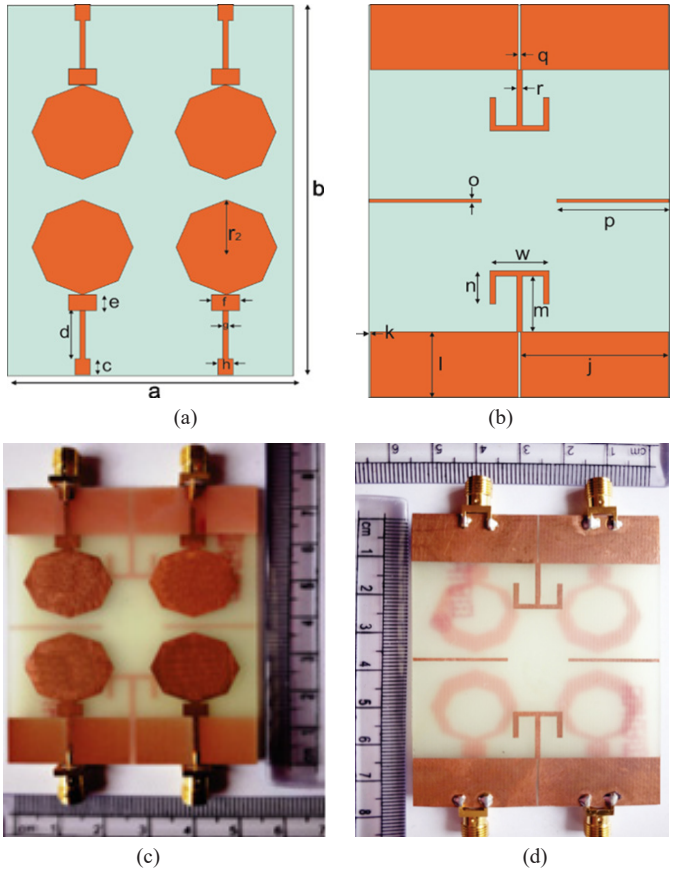
The design and construction of antennas serve as crucial pillars upon which the framework of contemporary connectivity is formed in the ever-expanding field of wireless communication. The search for effective and cutting-edge antenna solutions has taken on a level of significance never before seen as our world grows more and more dependent on smooth wireless connectivity [37]. "Antenna Design and Methodology" is a thorough investigation of the complex field of antenna engineering, revealing the ideas, procedures, and methodologies that guide the development of antennas for a variety of uses.

The frequency range, intended application, climatic circumstances, and design requirements are only a few of the variables that influence the material choice for antenna fabrication [38]. Electrical conductivity, dielectric characteristics, mechanical strength, cost, weight, and the unique needs of the antenna design and application all play a role in the material choice. To choose the best materials for their antenna projects, engineers and scientists frequently run simulations, verify their hypotheses, and optimize their choices. A typical substrate for PCB-based antennas is FR-4. It is affordable, widely accessible, and appropriate for lower-frequency applications. The electronics industry uses FR-4, an abbreviation for "Flame Retardant 4," extensively, particularly for printed circuit boards (PCBs). It is renowned for its mechanical tough-ness, flame-retardant qualities, and electrical insulating qualities.

The proposed prototype is demonstrated in Fig. 1 and its optimized parameters size is given in Table 1. The fabricated material is chosen as FR4 having thickness, permittivity and loss tangent of 1.6 mm, 4.4 and 0.02 respectively. Fig. 2 explains the design stages adopted for antenna element. The MIMO antenna geometry consists of four identical copies of a stepped microstrip line fed octagonal monopole with partial ground plane. Two elements are

Table 1.
Optimized Antenna Dimensions In Mm.

Design Parameter	a	b	c	d	e	f	g
Size	60	76	3.30	9.90	3.26	5.40	1.04
Design Parameter	h	i	j	k	w	m	n
Size	2.92	12.62	27.02	0.24	10.80	10.80	5.4
Design Parameter	o	p	q	r	r2		
size	0.62	20.43	0.48	1.02	9.71		



(a) (b)

(c) (d)

Fig. 1. Designed MIMO antenna (a) schematic of proposed antenna front view (b) schematic back view (c) fabricated picture front (d) fabricated picture back.

arranged adjacent to each other (spatial diversity configuration) and remaining two elements are placed in mirror configuration to the first two elements (mirrored along x-axis). To increase the isolation between the adjacent ports, folded T-shaped stubs are used to connect the adjacent ground planes. In case of directly opposite ports, parasitic elements are used. The total footprint for the designed MIMO antenna substrate is 60×76 mm^2.

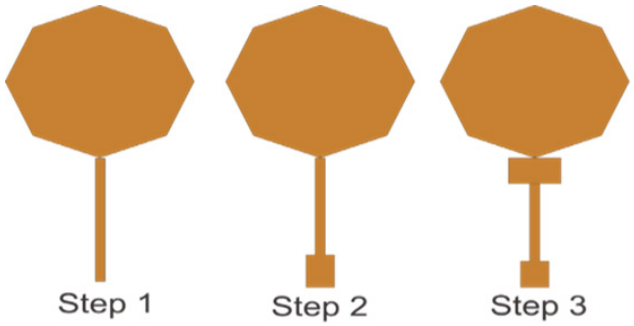


Fig. 2. Design steps diagram of antenna.

III. Results And Discussion

The design steps reflection coefficients are illustrated in Fig. 3. One can observes that the design stages 1 to 3 have an operating frequency range of 3.40-5.50 GHz, 3.40-4.40 GHz, and 3.10-4.60 GHz respectively. The folded T-shaped isolating structure gives isolation more than 12 dB and it's also connecting both ground plane. The isolation between the directly opposite ports and diagonally opposite ports is observed to be more than 12 dB and 16 dB respectively. In addition to isolation enhancement, folded T-shaped stubs and parasitic elements resulted into shifting of frequency lower side while higher side it remains same, thus results in wider frequency band. The presented results also show the frequency band is significantly higher in the S-parameter with T-shaped structure than in the one without. The frequency moves from 3.80 GHz to 2.40 GHz, and the whole operating band from 3.1-4.6 GHz to 2.16-4.30 GHz, leading to antenna shrinkage.

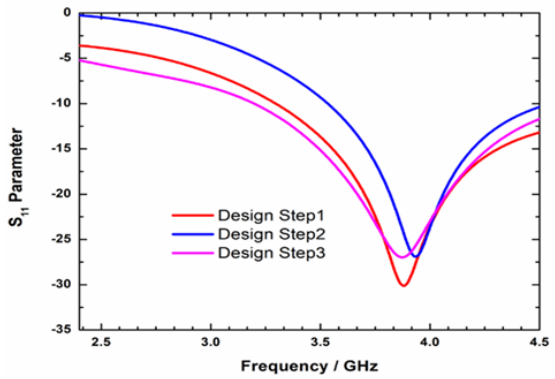


Fig. 3. Design steps results using S_{11} Parameter

The return loss and isolation with and without use of PE and folded T-shaped stub are illustrated in Fig. 4. It shows the better isolation and return loss using PE element and T shaped stub, while without parasitic element and T-Shaped stub (WPE&T) has good isolation between port 1-4 only. The presented results clear the use and effects of PE and T-Shaped isolating structure.

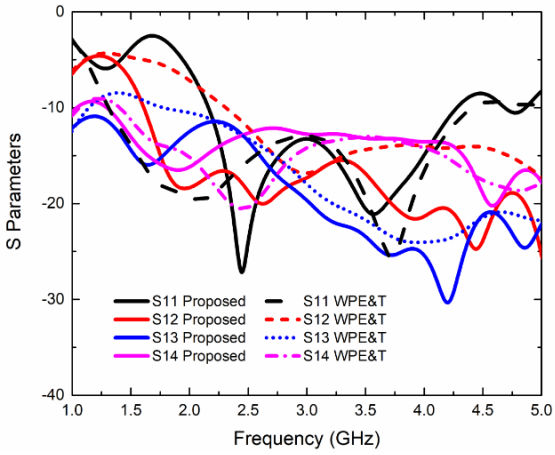


Fig. 4. Scattering parameters with and Without PE & T-shaped Stub (WPE&T).

The outcomes of the measured and simulated S-parameters are displayed in Fig. 5. The frequency range is 2.16 GHz to 4.3 GHz. The slight variation between the simulated and measured S-parameters may be seen. The reported findings further demonstrate the good isolation performance of the suggested design across the whole band.

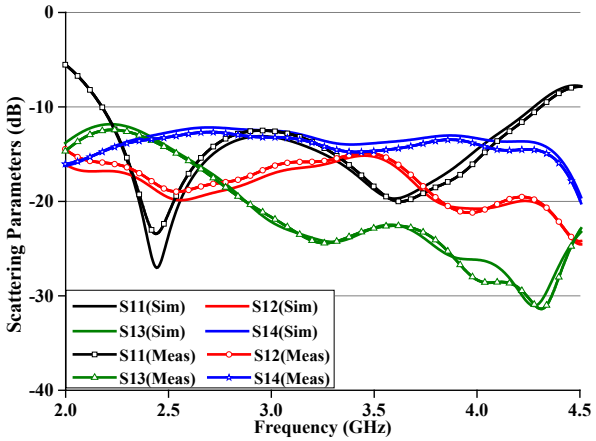


Fig. 5. Simulated and measured Scattering parameters

Surface current distribution measures the amount of current on the surface. Fig. 7 depicts the distribution of current on the antenna's surface at both resonances. When antenna port 1 is energized, a large amount of power is getting coupled to other ports in non-existence of folded T-shaped stubs and PE (WPE&T). In the presence of folded T-shaped element and PE, the amount of power getting coupled to other ports is significantly reduced. The maximum surface current due to port 1 is either cancelled or transfer in other direction due to the both isolating elements. The both isolating elements provide good improvements in isolation as compare to design without PE&T.

Fig. 6 displays the S-parameter data, which indicate a higher side shifting of the resonant frequency at 3.7 GHz. The isolation

is poor as compare to non-connection ground thus the design with non-connecting ground is considered.

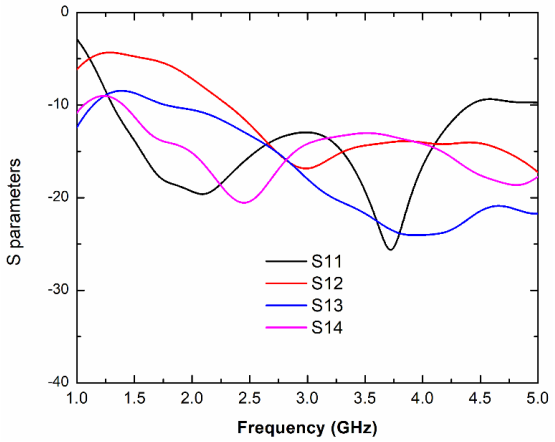
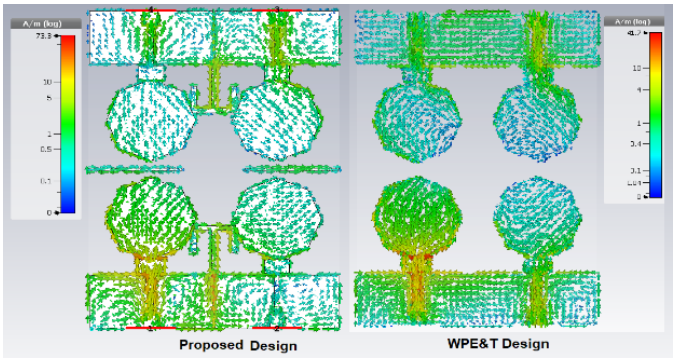
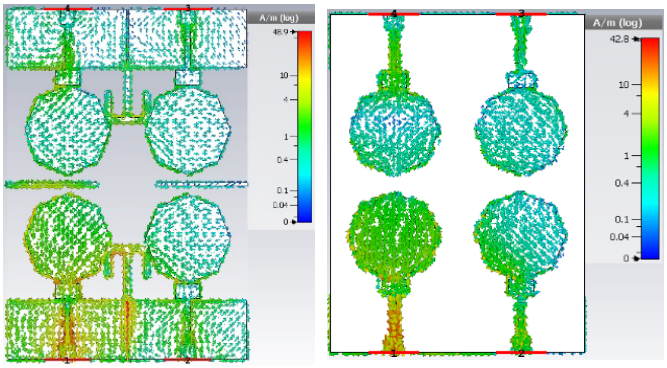


Fig. 6. Simulated Scattering parameters for connected ground.



(a) 2.40 GHz



(b) 3.59 GHz

Fig. 7. Graphical picture of surface current distribution.

The far field properties of any antenna for desired applications are one of the deciding parameters for effective design. The polar plot of E/H field is presented in Fig. 8. The polar plot shows the graphical behavior of distribution of energy. The major lobe radiation is found in the direction of 354°. Similarly polar plot of H-field shows the main lobe direction of 25°. The simulation and measured environment are slightly different thus small changes can be observed in both radiation patterns.

The gain shows the radiation ability of antenna in given direction. The gain and efficiency are the two basic parameters which show the suitability of antenna in outside world. The gain and efficiency plot in the whole band are presented in Fig. 9. The gain of the antenna varies from 2.35-3.44 dBi. The simulated radiation efficiency ranges between 83 to 93%.

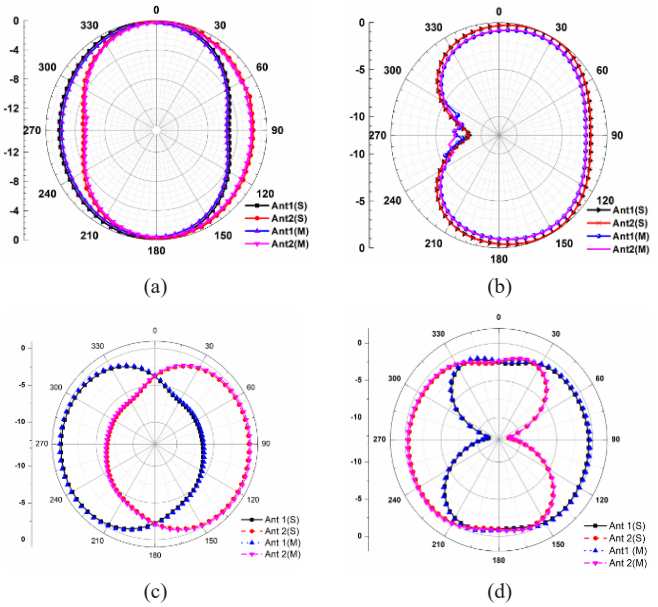


Fig. 8. Far-field characteristics (a) E-field at resonance 2.40 GHz (b) H-field at resonance 2.40 GHz (c) E-Field at resonance 3.59 GHz (d) H-field at resonance 3.59 GHz

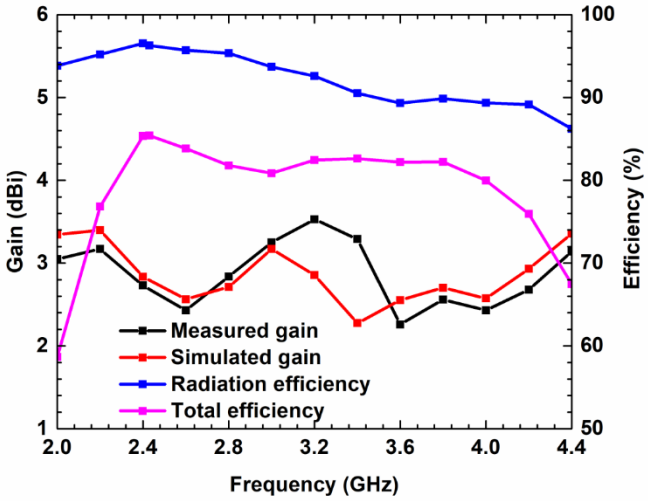


Fig. 9. Gain, total efficiency and radiation efficiency of proposed antenna.

One of the important performance parameters for any multi-element antenna system is its ECC characteristic. The Envelope Correlation Coefficient (ECC) can also be used to study isolation between the MIMO antenna's ports. A low ECC value—ideally zero—indicates greater isolation between the MIMO antenna's ports.

ECC plays a critical role in this regard. The calculation of ECC is done by given equation (1):

$$|\rho_e(i,j,N)| = \frac{\left|\sum_{n=1}^{N} S_{i,n}^{*} S_{n,j}\right|}{\sqrt{\left|\prod_{k(=i,j)} \left[1 - \sum_{n=1}^{N} S_{i,n}^{*} S_{n,k}\right]\right|}} \quad (1)$$

Where, total number of antennas are N and the antenna elements are i and j.

The ECC values calculated from scattering parameters are shown in Fig. 10. The ECC is < 0.03. It indicates the good diversity management. The good ECC is the guaranty of better performance in MIMO antenna.

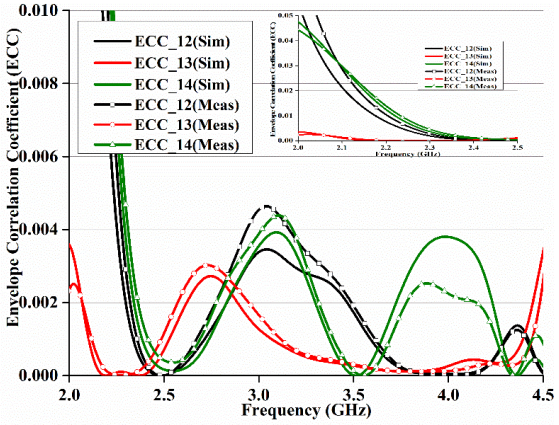


Fig. 10. Envelop correlation coefficient results.

Some indoor-outdoor characteristics of antenna are evaluated by parameter mean effective gain (MEG) in wireless channels. The MEG diversity parameter holds significance for MIMO antennas as it measures the proportion of power received by the MIMO antenna relative to the power received by the isotropic antenna.

The MEG determines average received signal strength of individual antenna. It is observed for both indoor applications at XPR= 6 dB and outdoor applications at XPR = 0 dB using equations (2) and (3).

$$\mathrm{MEG}_i = \frac{P_{\mathrm{rec}}}{P_{\mathrm{inc}}} = \oint \left[\frac{\mathrm{XPR}\cdot G_{\theta i}(\Omega) + G_{\phi i}(\Omega)\cdot P_{\phi}(\Omega)}{1+\mathrm{XPR}}\right] d\Omega, \tag{2}$$

$$\mathrm{MEG}_i = \int_0^{2\pi}\int_0^{\pi}\left(\frac{\mathrm{XPR}}{1+\mathrm{XPR}}\mathrm{G}_{\theta}(\theta,\emptyset)\mathrm{P}_0(\theta,\emptyset) + \frac{1}{1+\mathrm{XPR}}\mathrm{G}_{\emptyset}(\theta,\emptyset)\mathrm{P}_{\emptyset}(\theta,\emptyset)\right)\sin\theta d\theta d\emptyset \tag{3}$$

For evaluation of MEG, two mediums are considered i.e. isotropic and Gaussian. It is examined for certain cross polarization ratios (XPRs). The result is calculated for 0 and 6 dB of XPR. The MEG value is shown in Fig. 11 and listed in Table 2. MEG has a constant value of -2.90 dB for the isotropic case with XPR 0 dB, whereas it ranges between -4.1 dB and -4.8 dB for XPR 6 dB. Similarly, in the Gaussian situation, with XPR 0 and 6 dB, MEG has -3.10 to -4.10 dB and -6.10 to -7.0 dB. The MEG data at resonance are also presented in the table.

Table 2. Meg Of Isotropic And Gaussian Mediums

Resonance Frequency (GHz)	Medium			
	Isotropic (XPR in dB)		Gaussian (XPR in dB)	
	0	6	0	6
2.40	-2.94	-4.32	-4.12	-7.1
3.59	-2.94	-4.21	-3.92	-6.3

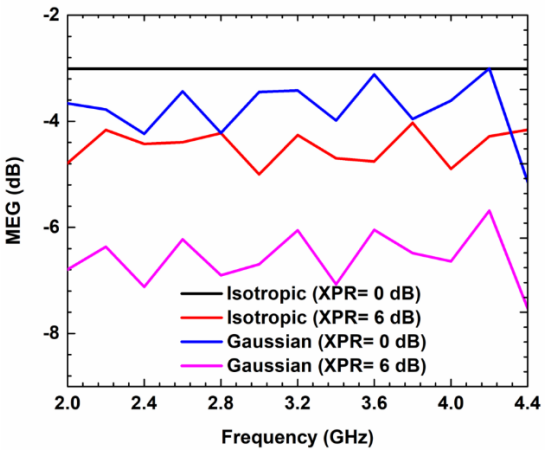


Fig. 11. MEG for Isotropic and Gaussian medium.

TARC is also a vital diversity parameter for multi element antenna system and array. The total return loss of the MIMO antenna array is known as TARC. TARC can be expressed mathematically as the square root of total incident power divided by the square root of total reflected power.

The TARC parameter is measured by Equations (4) and (5)

$$\Gamma = \sqrt{\frac{\text{received power} - \text{transmitted power}}{\text{received power}}} \tag{4}$$

$$\Gamma_{\mathrm{a}}^{\mathrm{t}} = \frac{\sqrt{\sum_{i=1}^{N}|b_i|^2}}{\sqrt{\sum_{i=1}^{N}|a_i|^2}} \tag{5}$$

Where [S]*[a] = [b]. The scattering matrix [S], excitation vector [a] and [b] are reflecting vector corresponding.

The complete return-loss of MIMO system is represented by TARC. It relates the incident power to the outgoing power in MIMO antenna. Fig. 12 displays the TARC curves at various excitation angles. The TARC bandwidth of 1.30 GHz is observed with best combination of 150°, 180° angles. The TARC bandwidth at different excitation angels is given in Table 3.

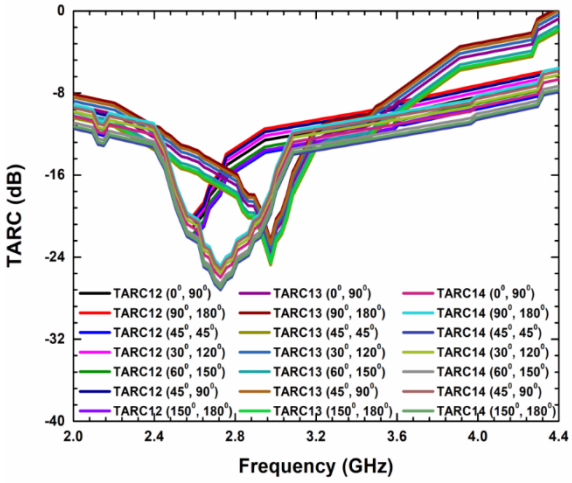


Fig. 12. TARC for different excitation angels.

Table 3. Tarc Bandwidth For Different Excitation Angles

Excitation angles (port 1-2, 1-3, 1-4)	Bandwidth (GHz) (port 1-2)	Bandwidth (GHz) (port 1-3)	Bandwidth (GHz) (port 1-4)
0^0, 90^0	1.1	1.2	1.1
90^0, 180^0	1.3	1.1	1.2
45^0, 45^0	1.2	1.2	1.2
30^0, 120^0	1.1	1.1	1.0
60^0, 150^0	1.0	1.1	1.1
45^0, 90^0	1.1	1.2	1.1
150^0, 180^0	1.3	1.35	1.38

The CCL and diversity gain also calculated for the proposed antenna. The Diversity gain (DG) result is specified in Fig. 13. The CCL is very important for message rate evaluation. The CCL limit is 0.4 bits/s/Hz [25]. In the suggested design, CCL is less than 0.4 b/s/Hz across the whole band. The CCL results are shown in Fig. 14.

DG can be computed by equation (6) which shows it is affected by correlation (ρ_e).

$$G_{DG} = 10 \times \sqrt{1 - |\rho_e|^2} \tag{6}$$

The calculation of CCL has been done by using the following given equation (7). It can be used to monitor system performance decline.

$$CCL = -\log_2 det(\eta) \tag{7}$$

where η is the correlation matrix

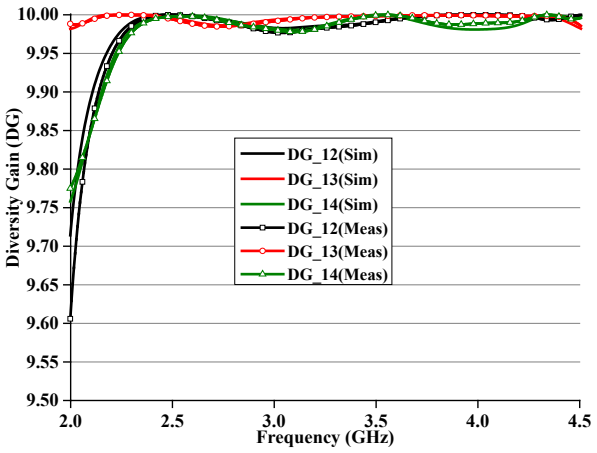


Fig. 13. DG of proposed MIMO antenna.

The amount of electromagnetic radiation (EM radiation) that communication antennas in wireless devices are permitted to create is measured by the specific absorption rate, or SAR.

Since the antenna is planned for wireless-applications, therefore the evaluation of its SAR is very necessary. Fig. 15 presents the human head model with proposed antenna placed near to head. The SAR values are calculated by averaging method IEEE/ICE 62704-1. As per ITU standard the value of SAR cannot be more than two watts per kilogram.

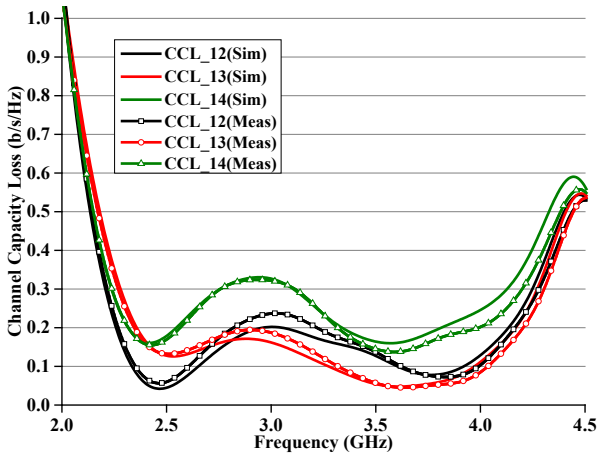


Fig. 14. results of CCL for proposed antenna.

Fig. 16 illustrates that the maximum SAR values near the human head for 10g and 1g are 7.52 nW/Kg and 8.83 nW/Kg respectively.

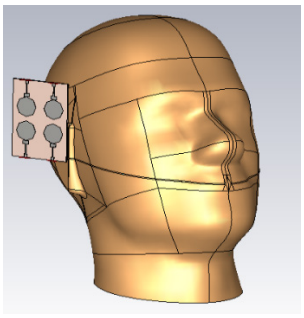
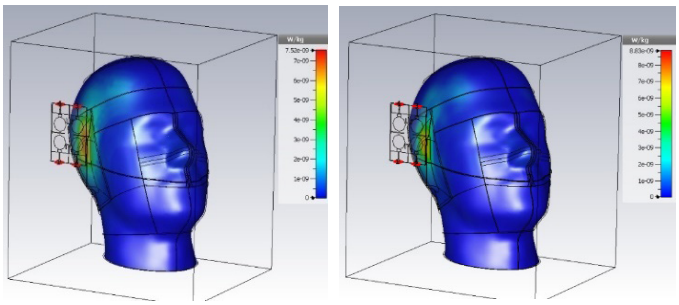


Fig. 15 Human head model with proposed antenna for SAR analysis



For10(g) (b) For 1(g)

Fig. 16 SAR analysis setup of proposed antenna.

The previously reported work and proposed work is compared on the basis of operating bandwidth, dimensions, ECC, isolation, peak gain, TARC and MEG in Table 4. The proposed design covers all frequencies band of WLAN and Wi-MAX. It has wider bandwidth than other antenna geometries. The size of the proposed design is also good and comparable to other designs. The values of MIMO performance parameters for proposed MIMO antenna are in acceptable limits.

Table 4. Proposed 2X2 Mimo Antenna And Previous Work Comparison

Reference	Frequency Band (GHz)	Size (mm^2)	ECC	Isolation at f_r in dB	Gain at f_r dBi	MEG (dB) at f_r
[16]	2.4-2.475	60 x 60	0.4	22	4	-
[19]	2.4-2.485	61 x 61	0.02	28	3.8	0.8
[21]	2.396-2.45	119 x 119	0.02	42	5.1	-
[22]	2.4-2.485	150 x 150	0.005	35	7.1	-
[31]	2.37-2.42; 3.33-3.90	70 x 60	0.01	25	1.8	-
[32]	2.34-2.56	72 x 72	0.01	12	2.0	3.0
[33]	2.24-2.50	56 x 37	0.08	10	2.0	2.5
[39]	2.12-2.15	120 x100	0.08	15	0.45	3.0
[40]	1.5–2.1	40 x 81.7	$5x10^{-3}$	17	1.0	3.0
[41]	2.18–2.50 5.33–9.06	88 x 31	--	--	3.5	--
Proposed	2.16-4.34	60 x 76	0.03	12	3.3	3.0

f_r =resonant frequency

IV. Conclusion

The creation of cutting-edge Wide-Band MIMO antennas shines as a beacon of progress in the ever-changing world of contemporary wireless communication, offering improved isolation and optimum performance. This investigation into the world of wide-band MIMO antennas has revealed the technology's transformative potential for a wide range of modern wireless applications. The main challenge in MIMO antenna design is the antenna coupling. The coupling degrades the performance of antenna i.e. efficiency, gain and isolation etc. Thus, proposed octagonal full shaped geometry based on four element design with T-shaped and PE for wide band of frequency has been proposed. In this design, two different approach is proposed for improving in isolation. The designed antenna produces improved isolation, acceptable MEG and TARC as per MIMO antenna needs, wide bandwidth, and good efficiency. For wireless communication CCL is also important parameter and it is found in acceptable limit while the SAR also shows the value under the limit. The designed MIMO antenna is fulfilling the modern antenna requirement.

Acknowledgment

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Hardware Acceleration of Singular Spectral Analysis: A Case Study on NQR Spectroscopy

K. Thulasiram Varma, Rangababu Peesapati, and Ch. V. Rama Rao

***Abstract*—Singular Spectral Analysis (SSA) is a computationally intensive approach to denoise and detect a time-series signal. It requires the evaluation of eigenvalues and eigenvectors of a covariance matrix, which is the computationally intensive step in the SSA algorithm. The current work presents a feasible approach to implement the algorithm in embedded hardware using a PYNQ-Z2 Field Programmable Gate Array (FPGA) board. We implemented the algorithm using both the Processing System (PS) and the Programmable Logic (PL) of the PYNQ-Z2 System on Chip (SoC) with the help of a High-Level Synthesis (HLS) tool. A case study is carried out on a Nuclear Quadruple Resonance (NQR) signal. The implementation result demonstrates a hardware acceleration of 15.48x with respect to the equivalent software implementation of the algorithm on the ARM Cortex-A9 processor.**

***Index Terms*—Singular Spectral Analysis(SSA), System on Chip (SoC), High-Level Synthesis (HLS), Pynq-Z2 Field Programmable Gate Array (FPGA).**

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I. Introduction

In the present-day scenario, data play a vital role in all applications. Many decomposition-based algorithms exist to extract meaningful information from a large amount of data. Singular Value Decomposition (SVD) is a technique that is popularly used in many domains, such as finance, medicine, image processing, computer vision, machine learning, and weather forecasting. Based on the principals of SVD, other feature selection algorithms, such as Principal Component Analysis (PCA), Independent Component Analysis (ICA), and Singular Spectral Analysis (SSA), were developed.

PCA transforms and projects the data into a new coordinate system. The set of new variables is called the principal components. The first principal component consists of maximum variance in the data, and the second one consists of reminding maximum variance orthogonal to the first principal component. Similarly, other principal components are derived. ICA is used in Blind Source Separation (BSS) problems, which helps to identify the origin of the signal sound in a mixed environment. The SSA algorithm specializes in decomposing the time series signal into trends, oscillations, and noise. All of the aforementioned algorithms are computationally intensive due to their reliance on matrix multiplication, eigenvalue computation, and inverse projection operation [1]–[3].

The primary motivation of this work is to reduce the computational complexity of the SSA hardware accelerator, which helps in trend extraction, noise reduction, and periodicity identification in large time series data. Applications range from financial forecasting to environmental monitoring and biomedical signal processing. The novelty of this work is twofold: implementing the SSA algorithm with the HLS approach using a covariance calculation of the Hankel matrix with a vectorial matrix multiplication with only upper diagonal matrix elements and further utilizing the power method to find the selective dominant eigenvalues and vectors for the reconstruction of the signal.

High-level synthesis (HLS) tools help developers to design hardware by describing the desired functionality with high-level languages such as C, C++, or SystemC rather than traditional hardware description languages (HDLs) like VHDL or Verilog. However, these HLS tools generate Verilog hardware. Furthermore, HLS provides advantages of improved productivity and seamless integration with the RTL and SoC framework, which find their applications ranging from cryptography and Internet of Things (IoT) to machine learning tasks and many more [4], [5]. The work explored the possibility of implementing the whole algorithm with a hardware-software co-design approach where signal reconstruction is performed on the Processing System (PS) side and matrix multiplication and eigenvalues and vectors computation was carried out on the Programmable Logic (PL) side. Intellectual property (IP)s were generated through the Vivado High-Level Synthesis (HLS) tools for the operations above. Further, these IPs were integrated into SoC's PL side. Hardware-software co-design on FPGA improves the overall system's throughput by exploiting parallel computation,

In addition, this paper presents a case study of the SSA algorithm and its hardware implementation on Nuclear Quadrupole Resonance (NQR) for denoising, trend, and periodicity identification. NQR signal processing is a non-invasive technique for identifying chemical substances [6]. This property has applications in the identification of narcotics and explosive materials. Acquiring a signal in an open environment filled with external noise and interference is challenging. To clean/denoise the signal and estimate the signal parameters, signal processing techniques and their hardware are essential.

We propose an SSA-based signal denoising approach in

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previous work [7] and observe a 32.4 dB improvement in signal quality in terms of SNR. In this paper, we carry forward the work and implement the SSA accelerator on FPGA hardware. The SSA hardware provides an acceleration factor of 15.48X, demonstrated compared to the software.

The related work on SSA implementations on FPGA is presented in Section II. The mathematical preliminaries of the SSA algorithm are explained in Section III. Section IV contains the proposed hardware architecture to implement the SSA algorithm on FPGA. Section V of this paper presents the results and discussion, followed by a conclusion and references.

II. Related works

Although the applications of the SSA algorithm and its variants are explored in the literature, very few works have been reported that implement the SSA algorithm on hardware such as FPGA. Huang et al., [8] implemented the SSA algorithm on the Hankel tensor using Tucker decomposition on various computational platforms such as Central Processing Unit (CPU), Graphics Processing Unit (GPU), and FPGA. Byun et al., [9], and his team extracted Auditory Evoked Potential (AEP) signals from the brain by eliminating multiple noises using SSA and ensemble averaging. Cyclone IV FPGA implemented the SSA algorithm with a 1 MHz operating frequency for signal extraction. 61.2% reduction in stimulus repetitions was observed, and the signal matching of 83.2% to the original was observed. The SVD portion of the SSA algorithm contains dominant signal singular values extracted using a one-sided Jacobi algorithm, which requires Coordinate Rotation Digital Computer (CORDIC) functions for trigonometric operations.

For eigenvalues and vector extraction of a matrix, mathematical approaches like Jacobi rotation, Lanczos-QR decomposition, and household transformation were studied and successfully implemented on different Field Programmable Gate Array (FPGA) to compute eigenvalues and eigenvectors of a matrix. Gleb et al., [10] developed two approaches to quickly multiplying the Hankel matrix with a vector. The Fast Fourier Transform (FFT) is applied to the auxiliary Hankel matrix and vector in the first approach. The drawbacks of this approach are loss of data due to cancellation errors. The second approach uses Karatsuba multiplication and observed lesser multiplication operations without data loss. Mohammad et al., [11] worked on the acceleration of PCA using High-Level Synthesis (HLS) on both Virtex 7 FPGA and Zed boards. Reported an improvement in the execution time and reduction in resource utility and power consumption compared to GPU, CPU and other works, and observed 0.67 ms execution time for 30x16 matrix with respect to Virtex 7 FPGA. Using the same approach of accelerating PCA on a Zed board, they observed an execution time of 0.44 sec with an operating frequency of 90 MHz on an image size of 640x480x12. Aysel et al., [12] implemented PCA on FPGA. In implementing PCA normalization, covariance matrix calculations and eigenvalue decomposition steps were performed using the Jacobi cycle-by-row method for the matrix size of 100×100. It uses the CORDIC algorithm to accelerate trigonometric and square root operations while implementing the Jacobi method on the FPGA. Based on the reported work [12], the authors implemented SSA using a Singular Value Decomposition (SVD) based approach, which performs principal components extraction that involves inversion and multiplication of the whole matrix. Further performing inversion operations for an entire matrix leads to increased resources and time-consumption of operation. The reported hardware SVD implementation consumes more than 121% of BRAM resources to implement a 100×100 matrix, which is not feasible. Although the literature suggests multiple works to implement Singular Spectral Analysis (SSA) using Singular Value Decomposition (SVD) and other approaches, there is a need to develop simple and computationally inexpensive methods to implement the SSA algorithm on FPGA. To overcome this problem, we proposed effective matrix multiplication, eigenvalue, and vector calculation approaches to extract the principal components of the 240×240 matrix.

III. Singular Spectral Analysis

SSA is a data-driven approach that decomposes time series signals into trends, oscillations, and noise using principal components [13]. The SSA algorithm has been used to remove artifacts and noise from biological signal processing [14]. It is also used in weather forecasting to find trends and seasonality in huge and dynamically changing weather data [15].

Fig. 1 shows that the SSA algorithm is divided into decomposition and reconstruction. The first stage of the algorithm internally consists of two steps: embedding the signal onto a Hankel matrix and identifying principal components. In the second stage of the algorithm, grouping and anti-diagonal averaging are performed to retrieve the desired signal in its original dimension [16].

The first step of the SSA algorithm is to embed the one-dimensional input signal onto a Hankel matrix, as shown in (1), where N is the length of the signal and window length $M = N/2$. Since the embed matrix $X^{'}$ is Hankel in nature, all anti-diagonal elements are the same.

$$X^{'} = \begin{bmatrix} X(t_1) & X(t_2) & ... & X(t_{N-M+1}) \\ X(t_2) & X(t_3) & ... & X(t_{N-M+2}) \\ ... & ... & ... & ... \\ X(t_{N-M+1}) & X(t_{N-M+2}) & ... & X(t_N) \end{bmatrix} \quad (1)$$

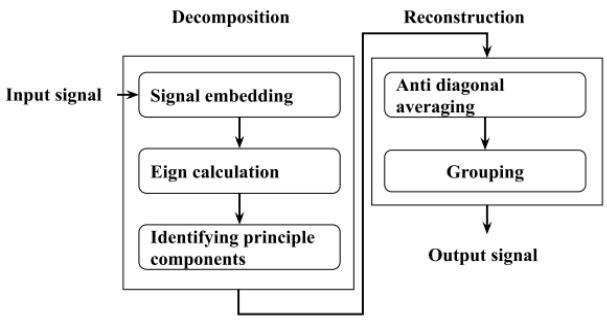

Fig. 1. SSA Flowchart.

Once the Hankel matrix is generated, to find the principal components (PC), the covariance of the Hankel matrix is calculated using (2), and from the covariance matrix, the eigenvalues (λ) and the eigenvectors (ρ) are computed.

$$C = (X^{'})^{T} * X^{'}/(N - M + 1) \tag{2}$$

$$PC = (X^{'}) * (\rho) \tag{3}$$

To obtain principal components, the eigenvalues and corresponding eigenvectors are sorted in descending order, and the eigenvectors are multiplied by the transpose of the embedded matrix as shown in (3).

The grouping step involves separating and summing similar principal components on the basis of the eigenvalues. Finally, the resultant matrix is inverted upside down after multiplying the PC matrix with ρ^{T}. In the last step of the algorithm, the sub-diagonal elements starting from $(N - M + 1) + n$ where $n = 1....N$ averaged, which results in an output signal of length N [13], [17].

IV. Hardware Implementation

The SSA hardware involves multiple levels of implementation and refinements. The algorithm is first computed at the software level using MATLAB and then translated to Python scripting language to run the algorithm on the Processing System (PS) of the FPGA. At this stage, profiling has been performed to find out the bottlenecks of computation and observed that out of three major parts of the algorithm, i.e. covariance calculation, eigenvalue and eigenvector extraction, and reconstruction. The matrix multiplication computation involved in the calculation of the covariance matrix consumes 91% of the total time on PS of the FPGA compared to the eigenvalue and vector extraction in other parts of the algorithm. Based on this, the implementation is split into two parts: lightweight and fast operations on PS and computationally intensive operations, which are converted into HLS and designed and integrated as hardware accelerators on the PL side of the SoC. In this approach, the covariance calculation, eigenvalue computation, and vector calculations are part of the algorithm on the accelerator on the PL and the reconstruction part of the algorithm on the PS. The entire design flow of the implementation is depicted in Fig. 2.

With the help of the Vivado High-Level Syntheses (HLS) tool, the code can be written in high-level C code to convert synthesized RTL sequentially and in a pipeline fashion with the help of pragmas. A custom SSA accelerator IP-core with computationally intensive operations is built to implement in the PL using (2)–(7).

As we can see from (2) for the calculation of covariance, the embedded matrix ($X^{'}$) is multiplied by its transpose and divided by the window length (M). To implement this equation and to fetch the vectors through DMA seamlessly, an optimal solution is proposed for computing matrix multiplication where only a one-dimensional vector is used, unlike the traditional matrix multiplication approach, where each row of matrix A is multiplied with every column of matrix B. Since the input Hankel matrix is symmetric in nature,

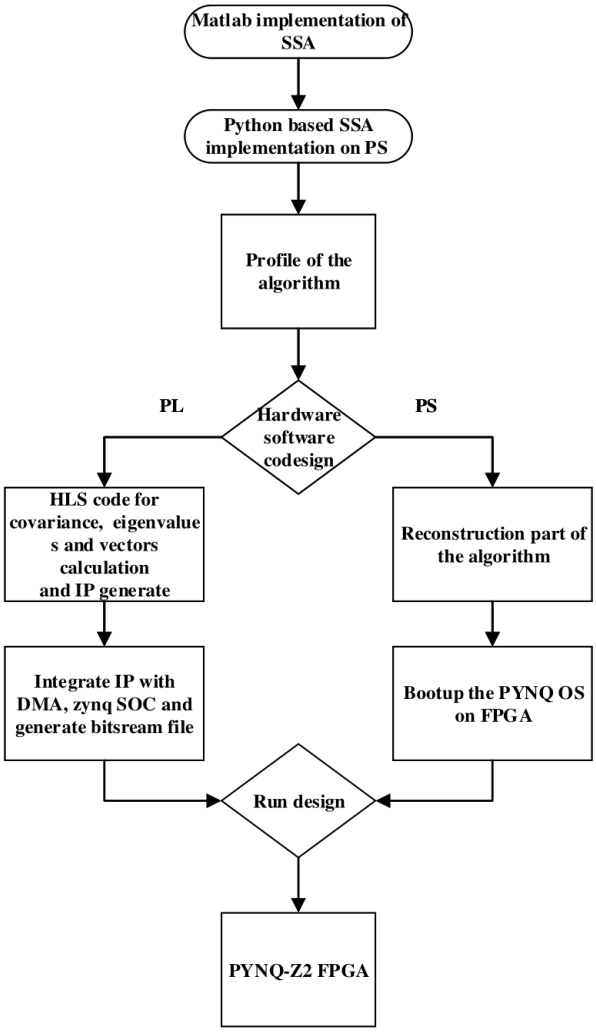

Fig. 2. Design implementation flow.

i.e., the upper triangle of the matrix is equal to the lower triangle, instead of calculating covariance for the whole matrix, only the upper triangle elements of the matrix are computed. The corresponding covariance is calculated. In this way, the computation is further reduced by the number of iterations and accumulation operations shown in Algorithm 1.

Once the covariance matrix is calculated, the power method is implemented as shown in Algorithms 2 and 3. The power method is an iterative approach to finding dominant eigenvalues and corresponding eigenvectors. This approach best suits the diagonal matrix obtained by performing the covariance calculation in the previous step. The power method begins with an initial guess of the dominant eigenvector, usually normalized all one vector as shown in (4) [18].

$$V = V_0/\left\|V_0\right\|_2 \quad V_0 = \begin{bmatrix}1 & . & . & . & 1\end{bmatrix}^{T} \tag{4}$$

Compute (5) to obtain new eigenvectors until the converging criteria is met. The eigenvalue for the vector is calculated using (6).

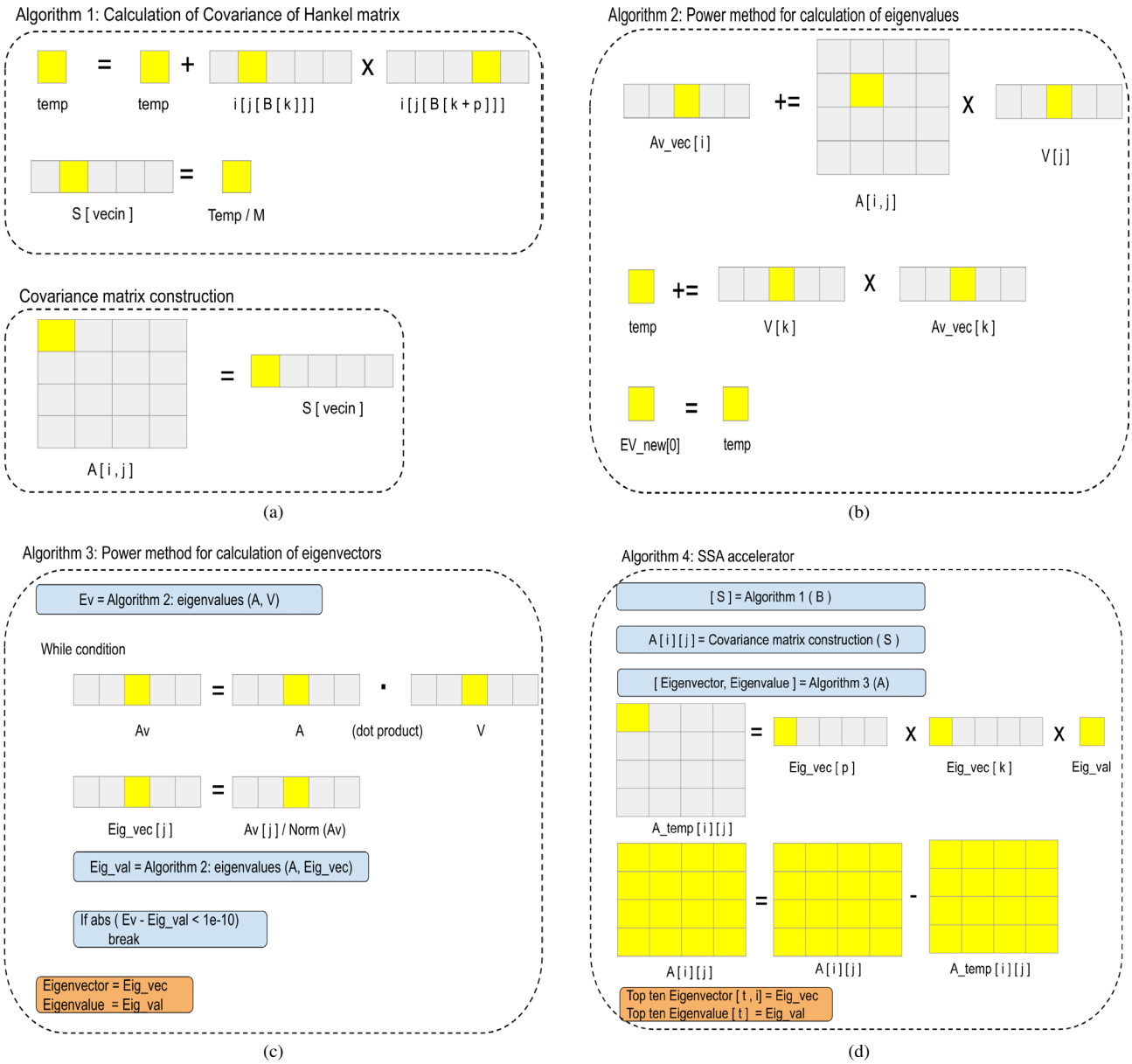

Fig. 3. (a) Algorithm 1: Covariance calculation and matrix construction, (b) Algorithm 2: Power method for calculation of eigenvalues,(c) Algorithm 3: Power method for calculation of eigenvectors,(d) Algorithm 4: SSA accelerator.

$$V_i = AV_{i-1} / \|AV_{i-1}\|_2 \tag{5}$$

$$EV = AV_i * V_i^T \tag{6}$$

The stopping criterion for the iteration is achieved when the difference between the new eigenvalue and the previous eigenvalue is less than 1e-10, i.e. $error = abs(EV - EV\_new)$.

$$A_{i+1} = A_i - EV * V * V^T \tag{7}$$

This eigenvalue computation involves the calculation of the second highest eigenvalue and eigenvectors, the product of the first highest eigenvectors and eigenvalue is subtracted from the main covariance matrix as shown in (7); likewise, the top ten eigenvalues and eigenvectors are calculated for this application, the same is depicted in Algorithm 4 [19], [20].

Fig. 3 illustrates the algorithmic implementation of a custom SSA IP core starting from the calculation of the multiplication of the covariance matrix and the construction of the resultant matrix in Fig. 3(a), the functional operation of the calculation of the eigenvalue and the eigenvector using the power method is shown in Figs. 3(b) and 3(c), and the complete top-level wrapper to calculate the top 10 eigenvalues and vectors is shown in Fig. 3(d).

V. Results and Discussion

The SSA algorithm is implemented on the PYNQ-Z2 FPGA board, which has a 650MHz ARM Cortex-A9 core processor with 512MB DDR3 RAM. The board includes 630 KB of fast

Algorithm 1 Calculation of Covariance of Hankel matrix

Input: B [L]
Output: S (Upper-triangle elements of the covariance matrix)

Ensure: $temp, i, io, p, vecin = 0; j, k = io$
  for all $i < M$ **do**
    for all $j < M$ **do**
      for all $k < M + io$ **do**
        $Temp = temp + B[k] * B[k + p]$
      end for
      $p = p + 1$
      $S[vecin] = temp/M$
      $vecin = vecin + 1$
      $temp = 0$
    end for
    $p = 0$
    $io = io + 1$
  end for

Algorithm 2 Power method for calculation of eigenvalues

Input : A[M][M], V[M]
Output : EV_new[vec]

Ensure: $temp, i, j, k = 0; vec = 1$
  for all $i < M$ **do**
    for all $j < M$ **do**
      $Av\_vec[i] += A[i][j] * V[j]$
    end for
  end for
  for all $k < M$ **do**
    $Temp += V[k] * Av\_vec[k]$
  end for
  $EV\_new[0] = temp$

Algorithm 3 Power method for calculation of eigenvectors

Input : A[M][M]
Output : Eig_vec,Eig_val

Ensure: $temp, norm\_temp, i, j, k = 0; vec = 1$
  for all $i < M$ **do**
    $V[i] = 1/sqrt(n)$
  end for
  $Algorithm\_2(A, V, EV)$
  while true **do**
    Av=A*V
    for all $i < M$ **do**
      $Temp += pow(Av[i], 2)$
    end for
    $norm\_temp = sqrt(temp)$
    for all $j < M$ **do**
      $Eig\_vec[j] = Av[j]/norm\_temp$
    end for
    $Algorithm\_2(A, Eig\_vec, Eig\_val)$
    if (abs(EV-Eig_val)<1e-10) **then**
      $Break$
    end if
    for all $k < M$ **do**
      $V[k] = Eig\_vec[k]$
      $Av[k] = 0$
    end for
    $EV = Eig\_val$
    $EV\_new\_out[0] = Eig\_val$
  end while

block RAM and 220 Digital Signal Processing (DSP) slices on the PL side. The experimental setup is shown in Fig. 4. The results are discussed with the help of a case study in the following subsection where SSA IP was used. The SSA IP is implemented sequentially and in a pipeline fashion. Further, floating and fixed point versions of the SSA IP on PL were explored.

A. Case study on NQR signal

Various spectroscopic methods, such as NMR, Raman, and Nuclear quadrupole resonance (NQR), are used to determine solid and liquid samples. They are used to evaluate the quality of agricultural and pharmaceutical products and to identify narcotics and explosive material [6]. Developing an efficient denoise algorithm and hardware implementation is essential to provide rapid time analysis. The case study implements the SSA algorithm to denoise the signal in less acquisition time than conventional averaging methods. The software-level implementation of the SSA algorithm is presented in the previous work [7]. In this current work, we implemented the same algorithm on the FPGA.

As shown in Fig. 5(a), the NQR signal of length 480 samples with different Signal to Noise Ratio (SNR), i.e. -5 dB,

Algorithm 4 SSA accelerator

Input : B[L]
Output : Eig_out[l]

Ensure: $ite, p, s, out\_l = 0; eig\_N = M + 1$
  $Algorithm\_1(B, S)$
  $A[M][M] = convertS[lo]$
  for all $i < ite$ **do**
    $Algorithm\_3(A, Eig\_vec, Eig\_Val)$
    for all $j < M$ **do**
      for all $k < M$ **do**
        $A\_temp[j][k] = Eig\_vec[p] * Eig\_vec[k] * Eig\_val[0]$
        $A = A - A\_temp$
      end for
      $p += 1$
    end for
  end for
  for all $l < M$ **do**
    $Eig\_out[l] = Eig\_vec[l]$
    $Eig\_out[l - 1] = Eig\_val[0]$
  end for

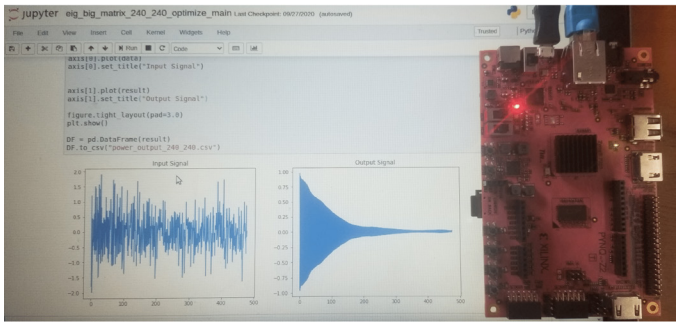

Fig. 4. Experimental setup.

0 dB and 5 dB, respectively, is generated in the PS with the help of (8),

$$S = A.e^{-t/T}cos(2\pi * Fc * t) \tag{8}$$

where Amplitude (A) = 1V, resonance frequency (Fc) = 10.25e4 Hz, sampling frequency (Fs) = 20.5e4 Hz and decay constants (T) = 0.5e-3 sec. The generated NQR signal is passed to the SSA IP core in PL with the help of Direct Memory access (DMA), where a covariance calculation module and power method module are built to extract eigenvalues and eigenvectors. The same is depicted in Fig. 6.

Figs. 5(c) and 5(d) corresponds to the dominant two eigenvalues and their eigenvectors of the covariance matrix; from this plot, it is evident that the first eigenvalue is the most dominant value for this signal; further, it is used for reconstruction of the original signal. The resulting eigenvalues and eigenvectors are appended into a one-dimensional array of 2410 samples of length and sent back to PS through DMA. The timing diagram in Fig. 7 provides a clear picture of data transfer from PS to PL via the master Advanced eXtensible Interface (AXI) stream bus. When the TREADY signal is high, TVALID is active for the duration of the data transfer (TDATA). TLAST specifies the last transaction of the data in the AXI stream protocol. The output eigenvalue was determined using covariance, eigenvalue, and vector calculation at the (IP) accelerator using Algorithms 1, 2, and 3. Further, the data were retrieved back to the PS using a slave AXI stream interface to reconstruct the denoised signal.

A comparison study is made with respect to resource utilisation and execution time between the sequential and pipeline approaches of implementing the algorithms on different signal lengths, and results are shown in Table I. From Table I, it is evident that the pipeline approach shows less amount of execution time compared to the sequential approach and further pipeline hardware consumes (BRAM-1%, DSP slices-12%, FF-43%, LUT-67%) higher resources than compared to sequential hardware while implementing the submodules of covariance calculation and power method on the PL side to extract eigenvalues and corresponding eigenvectors. From resources metrics, we can observe that for 512 sample signals, the BRAM utilisation is exceeded, so we considered a length of 480 sample signals. Apart from implementing the SSA algorithm in single-precision floating-point representation, fixed-point <29, 12> (29 total bits out of which 12 are integers, and the remaining 17 are fractional bits) were used for covariance calculation part of the algorithm and observed the reduction of resources utility in Flip Flops (FF) and Look-Up Tables (LUTs) in the order of 31.3% to 28% respectively as shown in Fig. 8.

Comparison is made between NQR signals with different SNR in Table II. From this table, we can observe that if the input signal power is more significant than noise, the time consumed by the system to execute the algorithm is less; this is due to the convergence rate of error while calculating the eigenvalues and vectors in PL. By referring to the input signal with 0 dB SNR in floating point (pipeline) representation, the total time to implement the whole SSA algorithm using PL modules (Matrix multiplication, eigenvalue, and vector computation) and signal reconstruction modules at the PS side is 14.36 sec. Further, an investigation was carried out by implementing covariance matrix calculation and power method on the PS. The total time on PS alone to execute the software version of the SSA algorithm is 222.3 sec. These results show that with the help of PL, an acceleration factor of 15.48x is achieved. Root Mean Square Error (RMS) of 1.10e-5 is observed between the output signal obtained from PL-PS codesign and PS alone implementation. The results show that the proposed hardware architecture for covariance calculation and eigenvalues and eigenvectors extraction performs better than the software version.

To check the feasibility and performance impact of the proposed approach on different FPGAs, we replicated the entire approach on the larger FPGA, i.e., ZCU104; the results indicate the reduction of hardware resources with improved performance. The hardware implementation of the algorithm on ZCU104 consumes 33% of BRAM, 6% of DSP, 11% of FF and 19% of LUT, and the total execution time is reported as 15.26 sec with both PL and PS in place. On PS alone, the algorithm requires 84.1 sec compared to 222.3 sec in PYNQ-Z2. However, the PS power consumption of the ZCU104 board is higher compared to PYNQ-Z2. ZCU104 consumes 2.63 watts compared to 1.25 watts on PYNQ-Z2. The compactness and power consumption criteria for the proposed algorithm of PYNQ-Z2 are best fit for portable and remote applications with limited power resources. However, for a larger signal reconstruction, ZCU104 is helpful because of PL RAM.

$$FOM = [(LUT + FF) * 8] + [(BRAM + DSP) * 16] \tag{9}$$

Based on the BRAM, DSP slice, FF, and LUTs counts. The Figure of Merit (FoM) values are calculated for all the proposed approaches using (9), and corresponding values are shown in Table III. As the metric of resource utility, the FOM values of pipeline-based SSA on PYNQ-Z2 are higher than that of fixed-point implementation of the algorithm.

Table IV depicts the comparison between existing and proposed principal component extraction methods. The proposed approach is implemented on 480 samples of synthesized NQR signals. Principal component extraction is an intermediate step used in SSA to identify dominant principal components in a noisy signal.

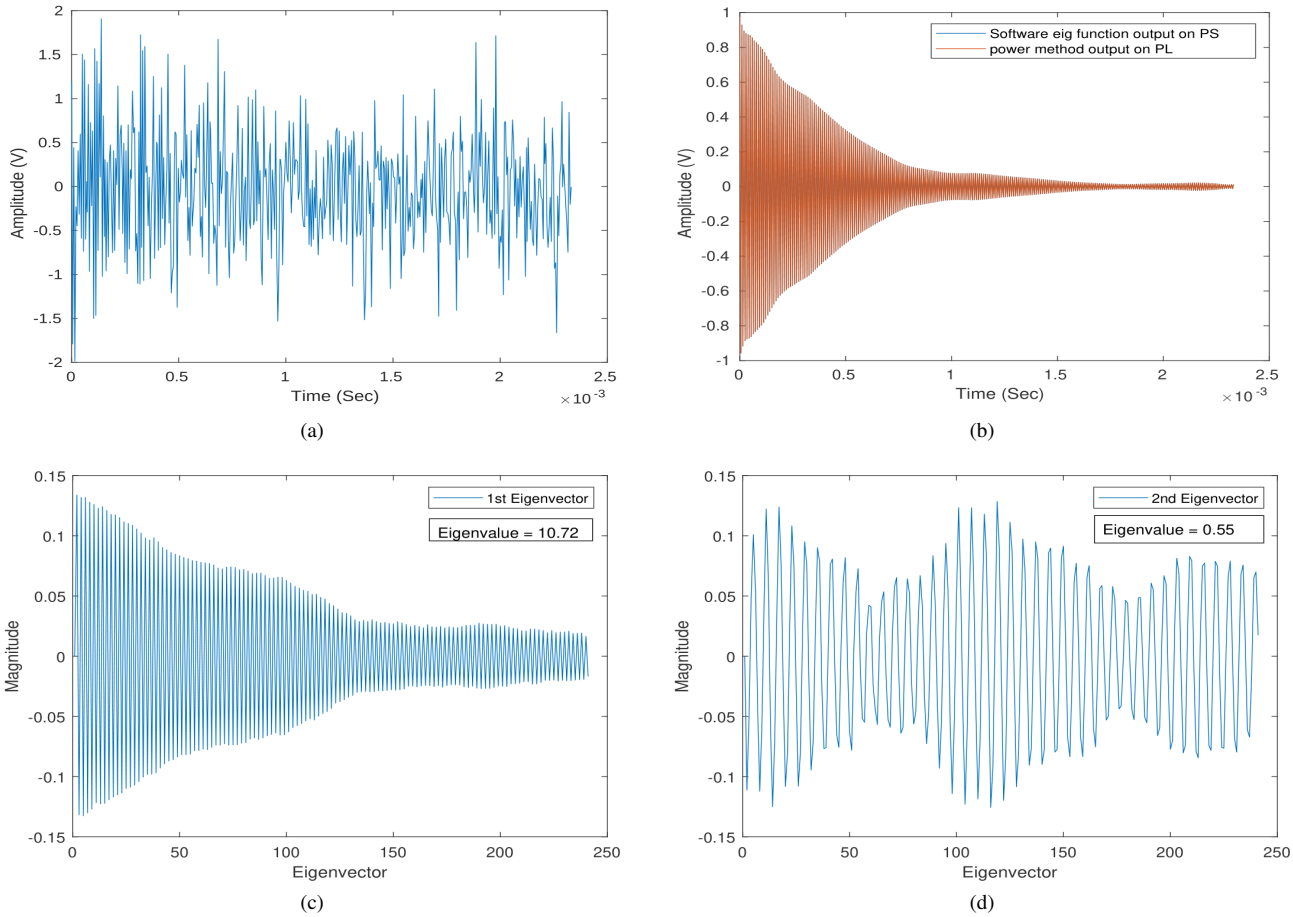

Fig. 5. (a) Noisy NQR signal (SNR=0 dB), (b) Denoised output signal (SNR=24.46 dB),(c) 1st Dominant eigenvalue and corresponding eigenvector,(d) 2nd Dominant eigenvalue and corresponding eigenvector.

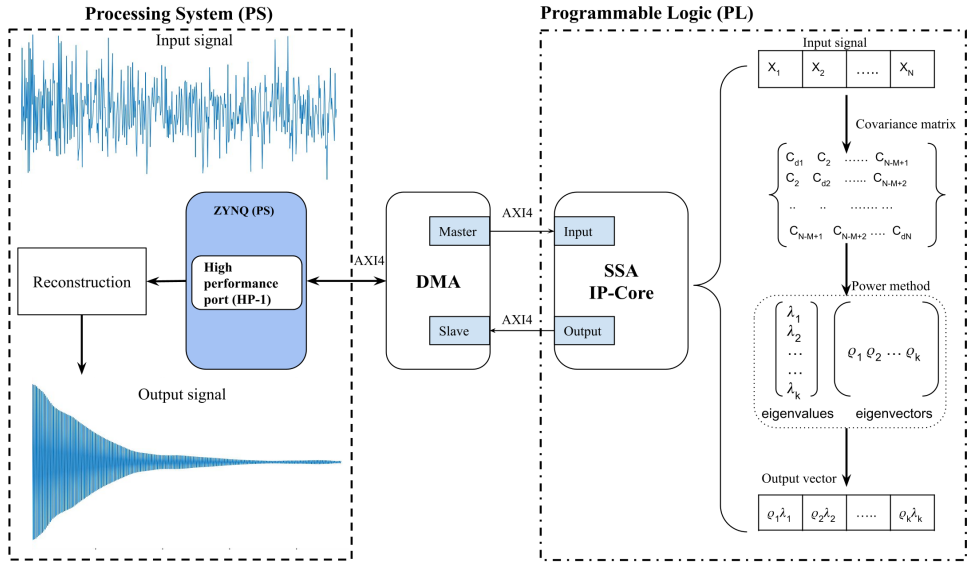

Fig. 6. Hardware design.

The SVD-based principal component extraction methods are faster than the proposed method. However, the proposed work contains overhead modules, such as matrix construction, which affects the overall speed. Furthermore, FoM of literature works [22], [23] shows that they consumed 2.1X and 3.4X higher resources than the proposed work.

In the future, we will work on a hybrid solution combining the proposed work and the SVD-based approach to extract principal components more effectively.

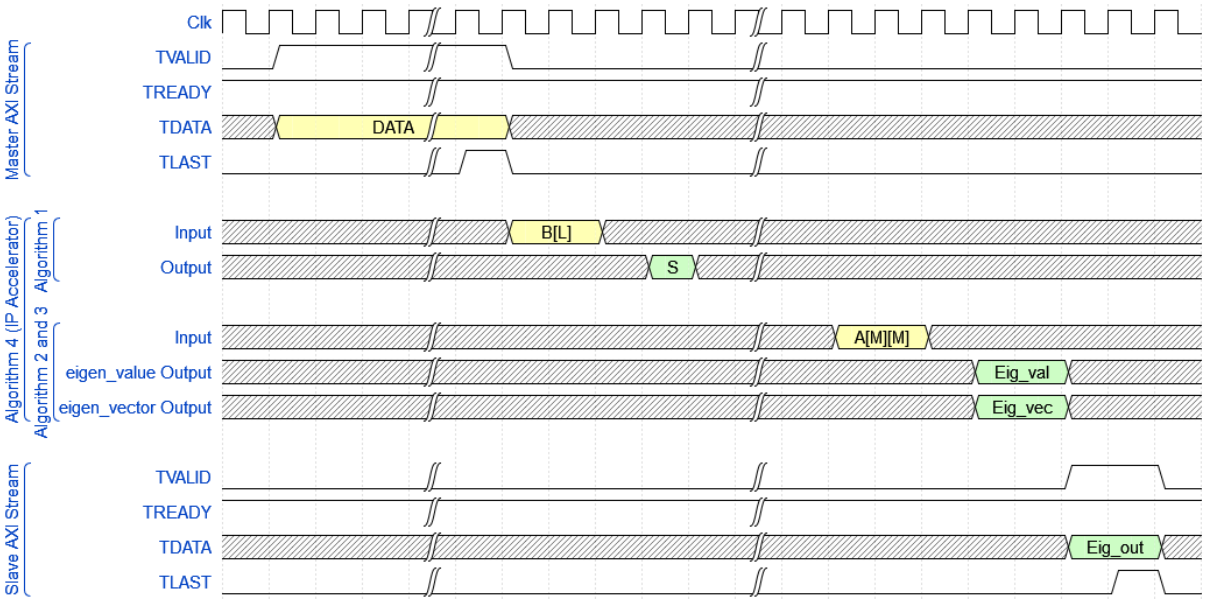

Fig. 7. Implementation timing diagram

TABLE I
RESOURCES UTILIZED IN COMPUTING SSA USING SEQUENTIAL AND PIPELINE APPROACHES

Resources	**Sequential Approach**	**Pipeline Approach**						
Signal Sample Length	**128**	**256**	**480**	**512**	**128**	**256**	**480**	**512**
BRAM_18K (%)	32	50	97	120*	33	51	98	121*
DSP48E (%)	42	42	42	42	48	48	54	48
FF (%)	23	23	24	23	36	46	67	68
LUT (%)	33	32	33	34	52	66	100	95
Execution Time (Sec)	5.16	12.82	25.93	-	3.83	8.44	14.36	-
Total Power (Watts)	1.78	1.82	1.98	-	1.94	1.98	2.18	-

* BRAM resources exhausted, not feasible to implement on the FPGA.

TABLE II
COMPARISON BETWEEN DIFFERENT INPUT SIGNALS IN TERMS OF SNR AND EXECUTION TIME

Input signal SNR (dB)	**Output signal SNR (dB)**	**Floating point sequential approach execution time (sec)**	**Floating point pipeline approach execution time (sec)**	**Fixed point pipeline approach execution time(sec)**	**Floating point PS implementation of the algorithm (sec)**	**Acceleration factor (PS implementation /Floating point pipeline implementation)**
-5	20.90	33.79	17.72	18.10	226.56	12.78x
0	24.46	25.93	14.36	14.99	222.31	15.48x
5	29.51	24.60	13.90	14.69	221.70	15.94x

TABLE III
IMPLEMENTATION OF SSA ON PL WITH DIFFERENT DATA TYPES

Approach	**RMS error w.r.t PS output**	**FOM***	**Static Power (Watts)**	**Dynamic Power (Watts)**
Floating point on PL (Sequential)	$1.10e^{-5}$	357328	0.16	1.82
Floating point on PL (Pipeline)	$1.10e^{-5}$	1006688	0.17	2.01
Fixed point on PL	$1.18e^{-5}$	706272	0.16	1.95

*Figure Of Merit (FOM) refer to (9).

TABLE IV
COMPARISON BETWEEN EXISTING AND PROPOSED PRINCIPAL COMPONENT EXTRACTION METHODS

Work	Platform	Matrix size	Execution time (sec)	FOM
[21] SVD on Reconfigurable System	Spartan-3E XC3S500E (50 MHZ)	40x40	0.48	73976
[22] Scalable FPGA Engine for Singular Value Decomposition	ZC706 (150 MHz)	200x200	0.01	2127120
[23] BCV Jacobi Algorithm SVD Solver	XC7V690T-3FFG1761 (200 MHz)	256x256	0.01	3425944
[Proposed work] SSA on NQR signal	PYNQ-Z2 (100 MHz)	240x240	14.36	1006688

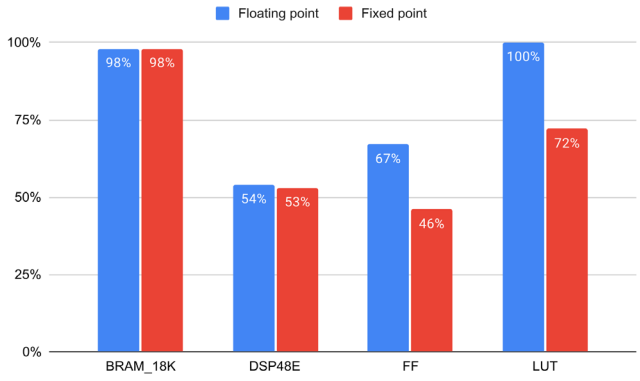

Fig. 8. Floating point and fixed point resource utility chart.

VI. Conclusion

Computationally effective Hankel matrix multiplication and desired eigenvalues and eigenvectors extraction are proposed for denoising the NQR signal. Overall, an optimal solution for implementing the SSA algorithm on the PYNQ-Z2 FPGA board is presented in this paper. An acceleration factor of 15.48x is observed while implementing the SSA algorithm on PL for covariance matrix calculation and eigenvalues and eigenvectors extraction, and PS for performing the signal reconstruction portion of the algorithm. Further, fixed-point implementation results suggest a reduction in the resource utility of the algorithm.

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Improving the Gain and Bandwidth of CMOS Circuits with Fe-MgO Tunnel Junctions

Mayank Chakraverty and Valayathoor N. Ramakrishnan

***Abstract*— This paper reports the influence of magnetic tunnel junctions on the electrical response of an operational amplifier (op-amp) circuit. As a baseline, the pure-CMOS operational amplifier has been designed using the 180 nm semiconductor process technology from the Taiwan Semiconductor Manufacturing Company Ltd. and the test bench has been simulated to obtain circuit performance metrics like open loop gain, phase, bandwidth and phase margin. The introduction of a magnetic element can upset the electrical behavior and the same has been observed with the introduction of Fe-MgO tunnel junction on the baseline electrical behavior of the operational amplifier test bench. Possibilities of connecting the tunnel junction to the different nodes of the op-amp test bench have been explored and the consequent drifts in the electrical response have been studied in this paper. Furthermore, an attempt has been made to mirror the transistors in the op-amp circuit with tunnel junctions and the consequent electrical responses have been studied in this paper. Such a magneto-CMOS hybrid circuit configuration can be used for a wide range of novel applications that demand a higher packing density in limited die area.**

***Index Terms*— Ferromagnets, first principles, magnetic elements, MRAMs, tunnel junctions**

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I. Introduction

Magnetic tunnel junctions (MTJs) are tiny magnetic elements that have a wide range of applications [1]. They are made by depositing two thin films of ferromagnetic material that sandwich another thin film of an oxide or another form of insulator [1-3]. These devices serve as building blocks of magnetoresistive RAMs (MRAMs) where the data is written into the magnetization of the ferromagnetic film and spin dependent tunneling phenomenon governs the conduction mechanism [1, 3, 4]. Being non-volatile, the stored data stays in the magnetization of the tunnel junction as long as the magnetic alignment of the ferromagnetic film is not disturbed by an external field [22], [23]. The stored data is read by the control transistors connected to the tunnel junction [5], [6]. With two ferromagnetic thin films on top and bottom of the insulating oxide layer, this magnetic device can have two resistance states, the low, parallel state resistance (R_p) signifying the relative parallel alignment of magnetic moments of the two ferromagnets and the high, antiparallel state resistance (R_{AP}) signifying an antiparallel alignment of magnetic moments of one ferromagnet in relation to the other [1], [7]-[10]. Resistance switching from low to high state or high to low state is a characteristic property of these devices [1], [11]-[14]. The tunnel junction is usually represented by an equivalent circuit that has a resistor connected to a capacitor in parallel, as reported in [1], [15]-[18].

A tunnel magnetoresistance ratio (TMR) is typically defined, in terms of the junction resistances in the parallel and antiparallel magnetized states (R_p and R_{AP}, respectively) [1], to quantify the percentage change in the junction resistance. This is expressed in equation (1).

$$TMR = \frac{\Delta R}{R_{AP}} \times 100\% = \frac{R_{AP}-R_P}{R_{AP}} \times 100\% \quad (1)$$

The values of R_p and R_{AP} have been computed from the I-V characteristics of the Fe-MgO MTJ through First Principles Local Spin Density Approxiation (LSDA) bandstructure calculations. The geometry of the device employed for the bandstructure calculations has been used to estimate the MTJ capacitance value. The Fe-MgO MTJ employed for device level LSDA bandstructure calculations reports R_p to be 1279 Ohms while the value of R_{AP} is found to be 13.8 Mega Ohms [1]. These resistance and capacitance values have been used in the equivalent circuit comprised of a resistor and a capacitor, as derived in [1], that replicates the behavior of the MTJ in circuit simulations.

Based on such band structure calculations and the device geometry, the resistance (R_p and R_{AP}) and capacitance values for simulating a Fe-MgO tunnel junction in the form of an equivalent circuit have been derived [1], [19] and the same values have been used in this paper. In addition to integrating such tunnel junctions in MRAMs, the prospect of incorporating these tiny magnetic devices in CMOS based circuits and studying the impact of these nanoscale magnetic devices on the electrical response of the circuits has been a topic of interest [20], [21]. In this paper, the very popular operational amplifier circuit [24]

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has been chosen for such a study. Often known by the name op-amp, the operational amplifier is a device that is primarily used for voltage amplification [25], [26]. The design is such that, in between the output and input terminals, resistors and capacitors serve as external feedback components that are connected to the voltage-amplifying device [27]. By virtue of the many feedback topologies, whether resistive, capacitive, or both, the amplifier can perform a variety of different operations, hence the name "Operational Amplifier" [28]. The resulting function or operation of the amplifying device is decided by these feedback components. Parameters like open loop gain, phase, bandwidth and phase margin are critical to determining the electrical response of an op-amp circuit [29] and hence the op-amp test bench has been simulated to obtain the open loop gain, phase, bandwidth and phase margin, without the tunnel junction and then with the inclusion of the Fe-MgO tunnel junction.

II. Operational Amplifier Basics

An integrated circuit with the ability to amplify weak electric impulses is called an operational amplifier [30]. In general, there are two input pins and one output pin on an operational amplifier. Its primary function is to output the voltage difference between the two input pins after being amplified [30]-[32].

A linear integrated circuit (IC) with numerous terminals is all that is needed to create an operational amplifier [33]. Op-amps are voltage amplifiers that are intended to be used in conjunction with external feedback devices, such as resistors and capacitors, placed between the input and output terminals of the device. It is a high-gain electrical voltage amplifier that typically produces a single-ended output from a differential input. Because they are utilized in so many different consumer, industrial, and scientific applications, opto-amplifiers are among the most commonly used electronic devices in use today.

Op amps typically feature three terminals: an output port with low impedance and two high-impedance input ports. The non-inverting input is represented by a positive (+) sign, whereas the inverting input is indicated by a minus (-) sign. Operational amplifiers are helpful for a range of analog operations such as power, control, and signal chain applications. They function by amplifying the voltage differential between the inputs. The positive and negative terminals of a DC voltage source are connected to the V+ and V− power supply terminals, respectively. If the V+ and V− common terminals are not connected to a ground or reference point, the op-amp could be damaged by twice the supply voltage.

Op amps are associated with numerous significant features and aspects (refer to Fig. 1). A more thorough description of these traits can be found below.

The operational amplifier's gain attained without any feedback being applied to the circuit is known as the open-loop gain (designated as "A" in Fig. 1). This indicates that the loop, or feedback path, is open. With the exception of voltage comparators, an open-loop gain frequently needs to be extremely large (10,000+) in order to be useful on its own [34]. Input terminal voltages are compared by voltage comparators. Voltage comparators can drive the output to either the positive or negative rails even with tiny voltage differentials [35]. In closed-loop configurations, high open-loop gains are advantageous because they allow stable circuit behaviors across variations in process, temperature, and signal.

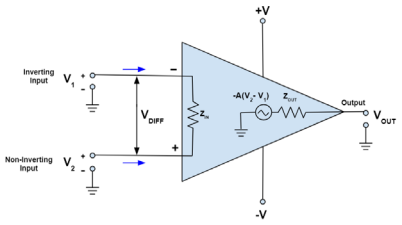


Fig. 1 Operational amplifier schematic

An ideal operational amplifier (op amp) would be able to maintain a high gain at any signal frequency and have an infinite bandwidth (BW). Nonetheless, every operational amplifier possesses a limited bandwidth, commonly referred to as the "-3dB point," at which the gain starts to decrease with an increase in frequency. The amplifier's gain then drops at a rate of -20dB/decade as the frequency rises. Higher BW op amps perform better because they can sustain higher gains at higher frequencies; however, this higher gain comes at the expense of higher power consumption or higher cost [36], [37].

Gain bandwidth product (GBP): GBP is a function of the gain and bandwidth of the amplifier, as the name implies [38]. Equation (2) can be used to calculate GBP, which is a constant value across the curve.

$$\text{GBP} = \text{Gain} \times \text{Bandwidth} = A \times BW \tag{2}$$

The frequency point at which the gain of the operational amplifier approaches unity is used to measure GBP. This is helpful because it lets the user figure out how much gain the device has open-loop at various frequencies. The GBP of an operational amplifier is typically a measure of its usefulness and performance because higher GBP op amps can be used to achieve higher frequencies with better performance [39].

Depending on the application and performance requirements, there are numerous other factors that could affect your design in addition to these primary ones when choosing an operational amplifier for any application. Supply voltages, noise, quiescent current, and input offset voltage are additional typical parameters [40].

Using an operational amplifier has a lot of benefits. Operational amplifiers are typically integrated circuits (ICs), are widely accessible, and have an endless range of selectable performance levels to suit the requirements of any application. Op amps are a vital component of many analog applications, such as comparator circuits, voltage buffers, filter designs, and many more, due to their wide range of applications [41]. Furthermore, before developing actual designs, most companies offer simulation support to designers, such as PSPICE models, to validate their operational amplifier designs. The fact that operational amplifiers are analog circuits and necessitate an understanding

of analog fundamentals like loading, frequency response, and stability are some of their drawbacks. Designing an op amp circuit that looks straightforward only to discover upon turning it on that it oscillates is a frequent occurrence. The designer usually needs to have moderate to high experience with analog design because of some of the important parameters that were previously discussed, and they need to understand how those parameters affect their design.

III. Related Works

Ever since the magnetic tunnel junctions have been found to be closely compatible with the current silicon-based manufacturing line, a lot of interests have spiked on integrating such magnetic elements into conventional CMOS circuits.

Simulation and fabrication of such magneto-CMOS hybrid circuits have widely been researched upon. In order to simulate such hybrid MTJ/CMOS circuits, G. Panagopoulos et. al [42] have introduced a SPICE-based framework. For hybrid MTJ/CMOS circuits developed entirely in SPICE, they have proposed a physics-based simulation framework that makes use of solely built-in components, like capacitors and voltage/current dependent voltage/current sources. Accuracy, quick simulation time, compatibility with current MOSFET SPICE models, simplicity of use, and ease of implementation are some advantages of this model. By enabling the exploration of performance tuning knobs at multiple levels of abstraction, from materials to the circuit level, the suggested framework closes the gap between materials, devices, and circuits. MTJ modeling in the proposed simulation framework incorporates spin-torque and an external magnetic field or fields and is based on the Landau-Lifshitz-Gilbert (LLG) equation. LLG is implemented using SPICE-integrated voltage-dependent current sources and capacitors, in addition to the heat diffusion equation, thermal variations, and electron transport. Because user-defined parameters govern the device dimensions, including MgO thickness and area, the suggested simulation framework is configurable. This model has been shown to correlate well with experimental data.

Using resistor-based temperature sensors (-55°C ∼ 125°C) and sigma-delta analog-to-digital converters (SD-ADC) as two case studies where high resistance is required and limits scaling down, the work done by Y.-a Wu et. al [43] exploits tunnel magnetoresistance-based replacement in reducing layout penalty of on-chip passive component during circuit design. Two temperature adaptive write schemes for MRAM are also suggested as additional uses for the suggested MTJ-based temperature sensor, considering the application in MRAM, the mainstream field of MTJ process, and addressing the issues of MRAM in wide temperature write operation. Major attributes associated with MTJ as the passive component, such as area, variation, and temperature characteristics, are covered in the study of these circuits. MTJ-based resistors are used in place of large CMOS resistance in SD-ADC and bridge transducer in resistor-based temperature sensors. Based on the simulation results, the resistor-capacitor (RC) integrator's passive resistor layout area was significantly decreased by 94.52% when compared to a completely 28nm CMOS design, or 94.13% for wide temperature application, while maintaining nearly the same performance. Furthermore, as compared to standard CMOS resistor-based temperature sensor designs, the MTJ-based bridge transducer in resistor-based temperature sensors can reduce the resistance layout area by more than 90% with improved linearity. The two distinct adaptive write circuits, which are based on the MTJ-based temperature sensor, aid in lowering the write power consumption and MRAM delay for wide temperature use, respectively. Furthermore, because MTJs are programmable, one can program their states to make the hybrid resistor's resistance changeable and controlled, giving it an advantage over a pure passive resistor. Therefore, it is possible to create a multimode circuit with switchable performance.

Adiabatic designs and logic-in-memory (LiM) structures that employ magnetic devices are two effective ways to achieve low power designs. This has been demonstrated by F. Sharifi et al. [44], by designing one-bit full adder circuits, AND/NAND, and XOR/XNOR circuits using a new adiabatic hybrid MTJ/CMOS structure. Synopsys HSPICE with 32nm CMOS technology has been used to model the designs, and they have been contrasted with non-adiabatic hybrid MTJ/CMOS circuits. Comparing the proposed XOR, AND, and full adder to the state of the art MTJ/CMOS full adder configurations, their respective power consumptions have been found to be nearly 13, 6, and 7 times lower.

IV. Baseline Simulation

To carry out the baseline simulation, an op-amp circuit has been designed using devices from the 180 nm semiconductor process technology from the Taiwan Semiconductor Manufacturing Company Ltd. (TSMC). A technology node in semiconductor manufacturing refers to the minimum feature size or critical dimension that can be produced on a semiconductor chip. It is typically measured in nanometers (nm) and represents the scale at which transistors and other components are fabricated on an integrated circuit. The technology node is a key parameter that determines the performance, power efficiency, and density of a semiconductor device. As technology nodes become smaller, more transistors can be packed onto a single chip, enabling increased processing power, faster speeds, and lower power consumption. Cadence Virtuoso schematic editor has been used to design the circuit and simulations have been carried out in Analog Design Environment (ADE-XL) using the SPICE models from TSMC. An important reason for selecting the 180 nm process node from TSMC is the stability of the process, proven record of better analog integration at 180 nm. Also, with 180 nm process, there is a possibility of obtaining higher sampling rates at lower power with smaller die sizes.

The schematic of the designed op-amp circuit is depicted in Fig. 2. The design parameter details have been summarized in Table I. The next step is to generate a symbol for the op-amp. Once the op-amp circuit has been fully rendered in its schematic form, the next essential step is to simulate it, to verify that it fulfills the specifications. The first step in testing a design is cre-

ating one or more test benches. A test bench is a schematic that includes the top-level schematic as a module and provides it with stimuli. The outputs of the design in response to the stimuli can be observed during simulation. To simulate the op-amp circuit depicted in Fig. 2, such a test bench has been built. This is depicted in Fig. 3.

TABLE I
DESIGN PARAMETERS OF BASELINE OP-AMP CIRCUIT

Inst	Parameters		Inst	Parameters
MP0	wt = 10um		**MP1**	wt = 10um
	l = 1um			l° = 5um
	ng = 1			ng = 1
MN0	wt = 25um		**MN1**	wt = 25um
	l = 3um			l = 3um
	ng = 2			ng = 2
	m = 2			m = 2
MN2	wt = 5um		**MN3**	wt = 5um
	l = 3um			l = 3um
	ng = 1			ng = 1
MN4	wt = 125um		**MP2**	wt = 210um
	l = 3um			l = 3um
	ng = 4			ng = 4
R0	R = 34.70kOhm		**C0**	C = 1,792pF
	l = 212um			w = 30um
	w = 2um			l = 30um
	s = 5			m = 4

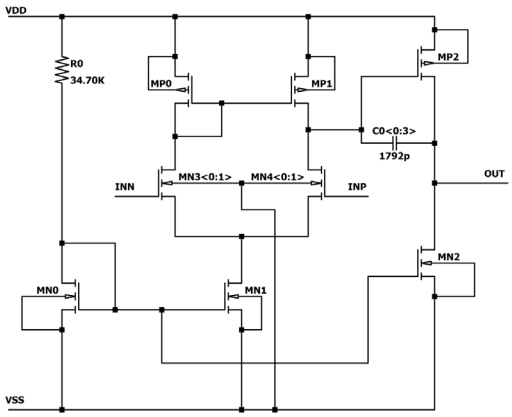


Fig. 2 Schematic of an op-amp circuit

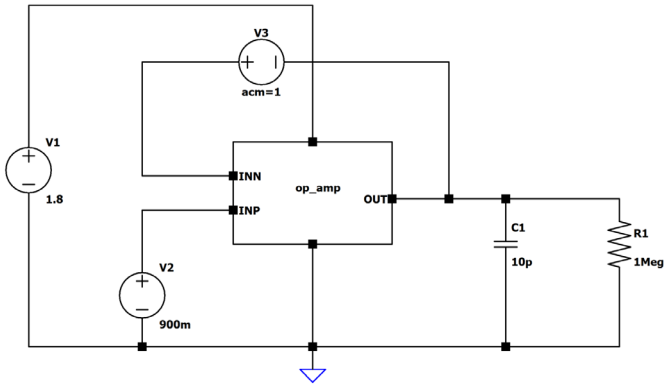


Fig. 3 Op-amp test bench (Baseline)

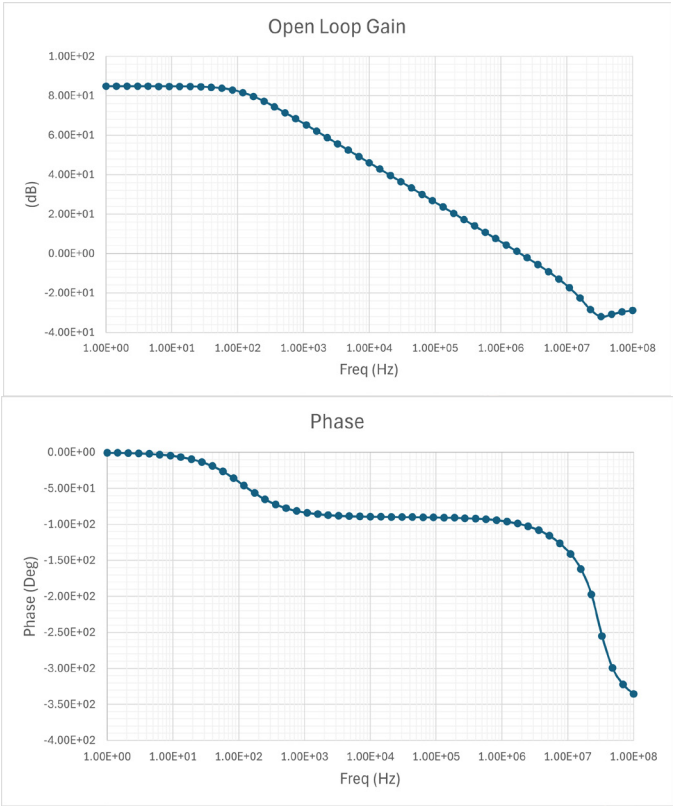


Fig. 4 Open loop gain and phase response from baseline op-amp simulation

The operational amplifier has been used in closed loop configuration and a test sinusoidal voltage source is inserted, setting AC Magnitude = 2.5V, Frequency = 10 kHz, connecting it to the input terminal INP. The VDD is set to 1.98V. The open loop gain and the phase response obtained from the simulated op-amp test bench of Fig. 3 is depicted in Fig. 4. In addition, the bandwidth and phase margin thus obtained are 127.7 Hertz and 79.81 degrees respectively.

V. INCORPORATING MTJS IN OP-AMP TEST BENCH

There can be several possible ways of connecting the magnetic element to the op-amp configuration. In this section of the paper, the focus has been on connecting the tunnel junction to the op-amp test bench circuit in a variety of ways and observing the drift in the circuit parameters and the electrical response. The aim of this work is to study the impact of such magnetic elements on the electrical behavior of pure-CMOS circuits like the operational amplifier but this can be termed a hypothetical approach, as there is no predefined application space that the hybrid circuit configuration can cater to. However, there are possibilities of applications of such magneto-CMOS hybrid circuits based on their electrical response. Such CMOS circuits with integrated Fe-MgO tunnel junctions could be applied in the industry for developing high-density, high-performance electronic components, such as advanced memory devices, sensors, and signal processing circuits. These hybrid circuits can offer enhanced gain, bandwidth, and reduced die area, making

them suitable for applications in telecommunications, data storage, and compact consumer electronics.

The first set of simulations has been carried out by connecting the tunnel junction to the INN node of the op-amp symbol. This is depicted in Fig. 5. Throughout this paper, the MTJ is depicted by connecting R_p (=1279 Ohms) in parallel with the MTJ capacitor, C. The R_{AP}, as reported in [1], is very high (13.8 Mega Ohms) and it has been observed that implementing the MTJ with R_{AP} and MTJ capacitor does not really impact the electrical response of the circuit under test. The corresponding bandwidth and phase margin have been computed, as tabulated in Table II, and the resulting open loop gain and phase response have been plotted, as depicted graphically in Fig. 10 and Fig. 11, respectively.

TABLE II
BANDWIDTH AND PHASE MARGIN OF MTJ BASED OP-AMP TEST BENCH

CIRCUIT TOPOLOGY	BANDWIDTH (HZ)	PHASE MARGIN (DEG.)
BASELINE	127.7	79.81
TOPOLOGY 1	584.1K	79.81
TOPOLOGY 2	584.1K	79.81
TOPOLOGY 3	584.1K	79.81
TOPOLOGY 4	659.7K	104.7
TOPOLOGY 5	673.4K	86.07

In the next variant of the circuit topology, the tunnel junction has been connected to the INP node of the op-amp symbol, as shown in Fig. 6, and the corresponding open loop gain and phase response are plotted in Fig. 10 and Fig. 11. The bandwidth and phase margin values thus computed can be found in Table II.

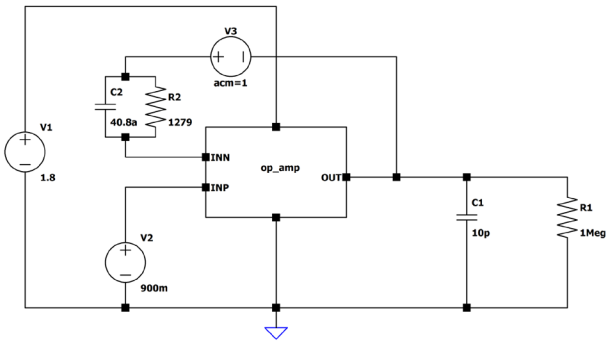


Fig. 5. Op-amp test bench with MTJ connected to INN (Topology 1)

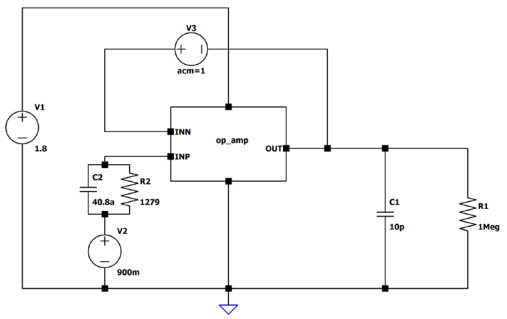


Fig. 6 Op-amp test bench with MTJ connected to INP (Topology 2)

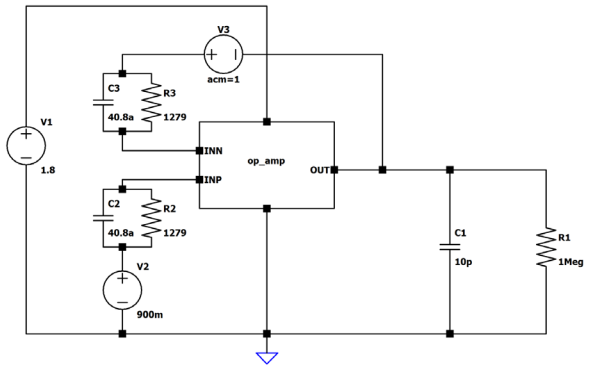


Fig. 7 Op-amp test bench with MTJs connected to INN and INP (Topology 3)

Unlike the two previous cases where the op-amp test bench has been simulated with a single tunnel junction, the next magneto-CMOS circuit topology has a tunnel junction connected to each of the two input nodes (INN, INP) of the op-amp symbol; the circuit is shown in Fig. 7. With two tunnel junctions in the design, the silicon area does not go up as the tunnel junctions are nanoscale, extremely tiny devices relative to the other components in the circuit. The open loop gain and phase response have been plotted in Fig. 10 and Fig. 11, respectively, and the bandwidth and phase margin have been computed as well, as presented in Table II.

Another couple of possibilities of a hybrid magneto-CMOS circuit can be with the tunnel junction connected to the OUT node of the op-amp symbol, and with the tunnel junction connected to the power (VDD) line of the test bench. This is depicted in Fig. 8 and Fig. 9, respectively.

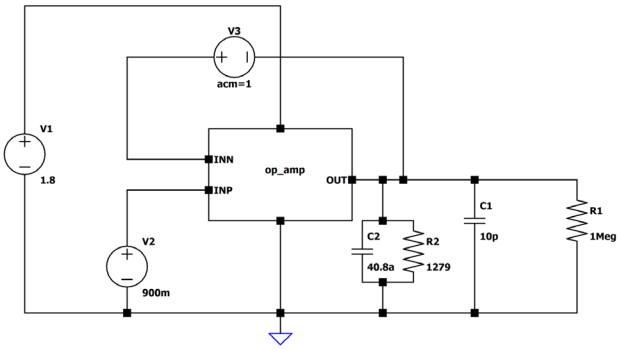


Fig. 8 Op-amp test bench with MTJ connected to OUT (Topology 4)

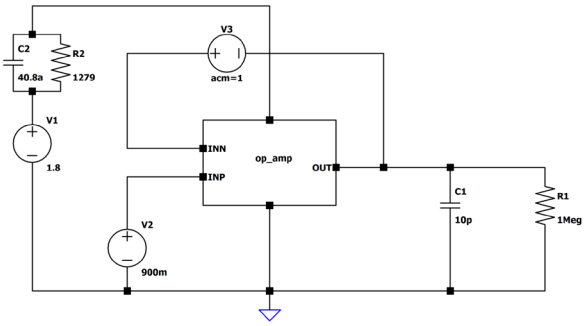


Fig. 9 Op-amp test bench with MTJ connected to VDD (Topology 5)

The primary purpose of an op-amp is to increase the input signal, and the functionality of the op-amp improves with an increase in the open loop gain. Open loop gain is defined as gain when there is no positive feedback nor negative input. Based on the simulation results obtained so far, connecting the op-amp to the tunnel junction in the manner that is depicted in topology 4 and topology 5 result in lower open loop gain, in comparison with the results obtained using topologies 1, 2 and 3.

Higher frequency signals can be amplified by the op-amp with a larger bandwidth, which results in faster speeds. The bandwidth of the op amp, in the electrical world, is the frequency at which the signal gain is 1/sqrt(2), or 0.707 of the ideal value. Op-amps can function with expected behavior up to this maximum frequency. It can be seen from Table II that the bandwidth and phase margin values obtained from the baseline test bench simulation are low as compared to the values obtained from simulation of op-amp test benches with tunnel junctions connected to either or both the inputs, at the output or even to VDD. In fact, there is a marked increase in the bandwidth as soon as the magnetic element is introduced into the pure-CMOS circuit. From this observation, a designer can conclude on using tunnel junctions in such CMOS circuits as op-amps to enhance the bandwidth and phase margin at the expense of extremely low die area overhead and this has a cost advantage as well.

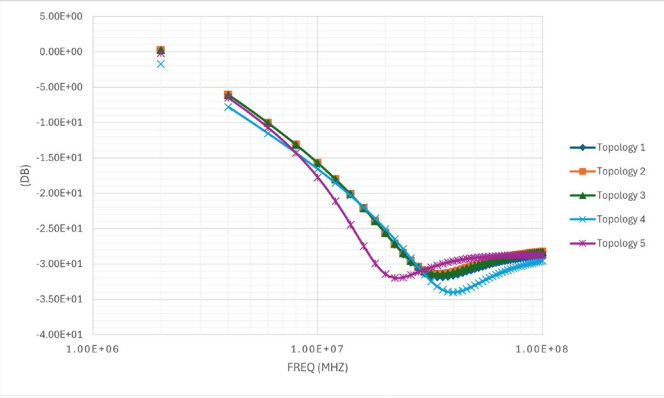


Fig. 10 Open loop gain of op-amp test bench with tunnel junctions

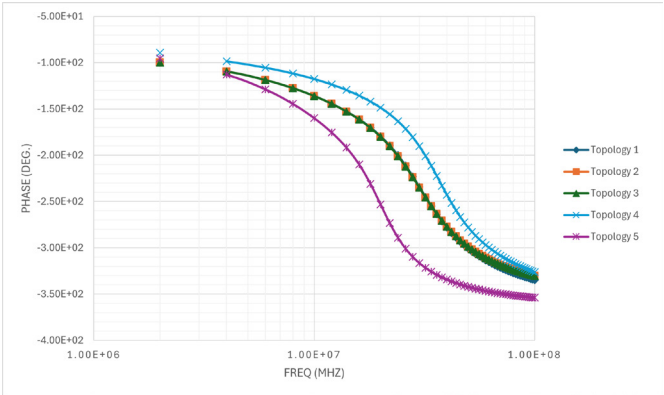


Fig. 11 Phase response of op-amp test bench with tunnel junctions

When the gain of the amplifier crosses 0dB, phase margin measures the degree of phase shift. Essentially, it serves as a gauge for how likely the system's second pole is to lead to instability. About a decade before the corner frequency, phase changes begin. Less than 180° of phase shift is required. The amplifier's real phase shift, measured in degrees, is the phase margin, which is 180°. Usually, anything above 45° is acceptable. System stability increases with phase margin. Reduced phase margin results from capacitive loading. In the simulation results reported so far, the topology 4 results in the highest phase margin followed by topology 5 while the remaining three topologies report a relatively lower phase margin.

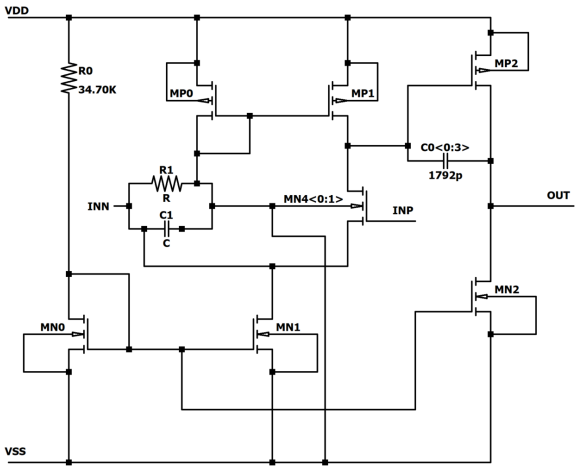
VI. MTJ Based Op-Amp Circuit Simulation

In this section of the paper, an attempt has been made to replace the transistors in differential pair used in the op-amp circuit depicted in Fig. 2 with the Fe-MgO tunnel junction and study the impact on the electrical behavior of the op-amp test bench. So, all the changes in the design have been done within the symbol hierarchy of the circuit and the baseline test bench of Fig. 3 has not been altered for simulation in this part of the work.

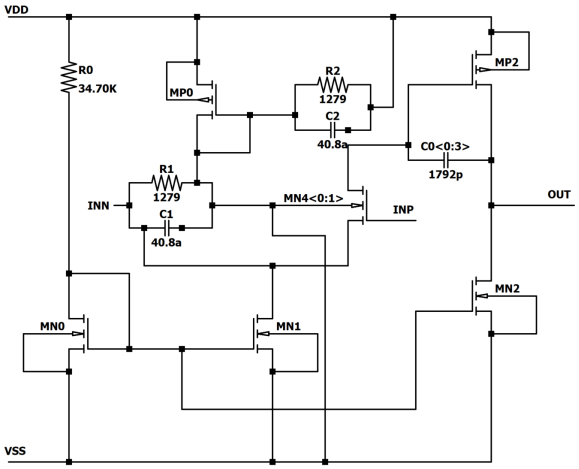
Replacing the transistors in the differential pair, one by one, has resulted in four op-amp circuit variations that have been simulated in this paper. This is depicted in Fig. 12 (a) – (d). A definite pattern has been followed while replacing the MOSFETs with tunnel junctions. For instance, the lower left NMOS transistor of the differential pair is the first device to be replaced by the Fe-MgO tunnel junction, followed by the estimation of bandwidth and phase margin along with simulating the open loop configuration of the corresponding test bench, thus obtaining the gain and phase as done in the previous section of the paper. As compared to the baseline simulation, i.e., with no tunnel junction involved in the op-amp configuration, the bandwidth and phase margin thus obtained are high. This behavior is again consistent with the results reported in the previous section of the paper, where the inclusion of a tunnel junction helped raising the bandwidth of the simulated circuit. Next, the diagonal PMOS device has been replaced by the magnetic element and the performance metrics have been obtained. In the third iteration, the other PMOS device in the differential pair has been replaced, followed by replacement of the only remaining NMOS transistor in the differential pair. The bandwidth and phase margin obtained from simulating each of the circuit iterations have been presented in Table III. While, the open loop gain and phase response of each circuit variation have been plotted in Fig. 13 and Fig. 14, respectively.

Another observation from the simulation results is that the highest bandwidth is reported by the op-amp circuit where all the transistors in the differential pair have been replaced by tunnel junctions. This highlights the role of tunnel junctions in raising the bandwidth of CMOS circuits with magnetic tunnel junctions as part of it. The corresponding phase margin is also high. The same circuit also reports the highest open loop gain, resulting in the highest gain-bandwidth product among all the circuits that have been simulated in this paper. The results in Table III are quite consistent with plots in Fig. 13 and Fig. 14 as the circuits with tunnel junction replacing the diagonal tran-

sistors, one by one, in the differential pair result in the same bandwidth and phase margin. From Fig. 13 and Fig. 14, it is seen that the same two circuits result in overlapping open loop gain and phase response.



(a)



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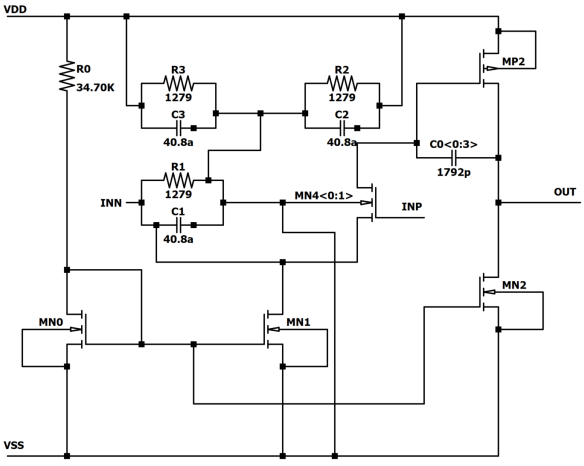
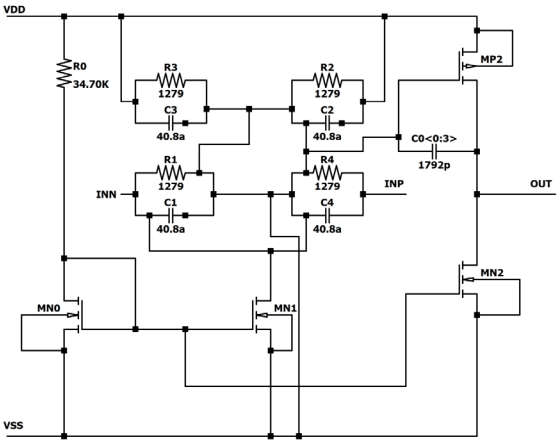


(c)



(d)

Fig. 12 Schematics of op-amp circuit with MTJs replacing NMOS and PMOS devices in differential pair

TABLE III
BANDWIDTH AND PHASE MARGIN OF MTJ BASED OP-AMP TEST CIRCUIT

OP-AMP VARIATION	BANDWIDTH (HZ)	PHASE MARGIN (DEG.)
NO VARIATION (BASELINE)	127.7	79.81
OP-AMP VARIATION 1	606.3K	93.19
OP-AMP VARIATION 2	588.4K	176.2
OP-AMP VARIATION 3	588.4K	176.2
OP-AMP VARIATION 4	657.5K	113.4

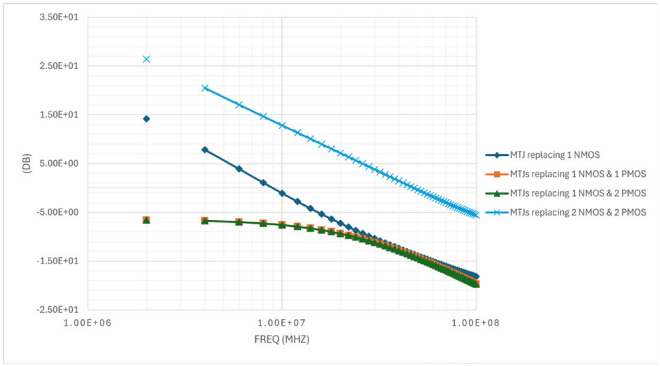


Fig. 13 Open loop gain of op-amp circuit with MTJs replacing NMOS and PMOS devices in differential pair

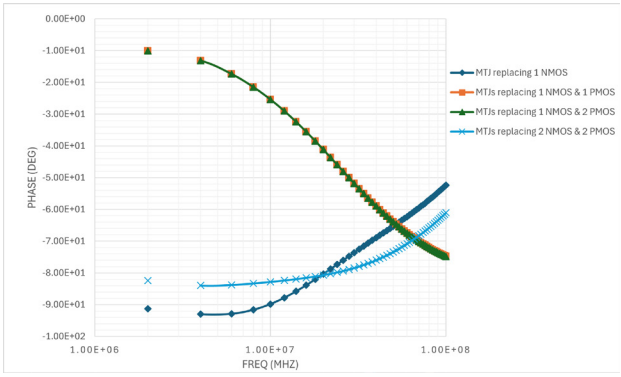


Fig. 14 Phase response of op-amp circuit with MTJs replacing NMOS and PMOS devices in differential pair

VII. Conclusions And Future Work

This paper has presented interesting results obtained from the simulation of a tunnel junction based operational amplifier. Two sets of simulations have been carried out. In the first set, the effect of adding a tunnel junction to the op-amp test bench has been studied and the electrical behavior has been compared with the simulation results of baseline op-amp test bench. In the next set, the transistors have been replaced by tunnel junctions, one at a time, followed by simulation of the resulting op-amp circuit. In both the sets of simulation, it is observed that the introduction of tunnel junction increases the bandwidth and the phase margin of the circuit, the open loop gain also improves with the addition of tunnel junction as compared to the baseline op-amp simulation. The results from the magneto-CMOS op-amp circuit simulation open up such hybrid circuits for many applications that require high gain bandwidth product while consuming very little die area as the tunnel junctions with nanoscale device dimensions do not add to area overhead but do influence the electrical behavior of pure CMOS circuits in a positive direction.

The plan is to take this work forward to the next stage and attempt to fabricate such a magneto-CMOS circuit on silicon and characterize the circuit to obtain real electrical response of the hybrid circuit based on measured silicon data.

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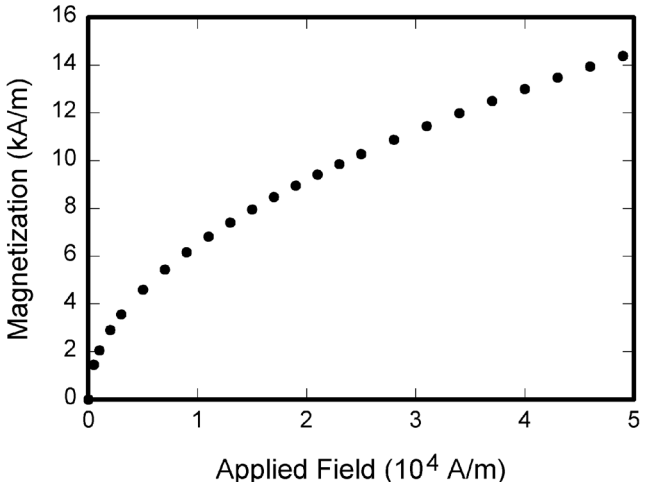

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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If you are using *Word,* use either the Microsoft Equation Editor or the *MathType* add-on (http://www.mathtype.com) for equations in your paper (Insert | Object | Create New | Microsoft Equation *or* MathType Equation). "Float over text" should *not* be selected.

IV. Units

Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception

TABLE I
Units for Magnetic Properties

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb $= 10^{-8}$ V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T $= 10^{-4}$ Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 $= 10^{-3}$ J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	$1 \rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	$1 \rightarrow 4\pi \times 10^{-7}$ H/m $= 4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	$1 \rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

V. Helpful Hints

A. Figures and Tables

Because we will do the final formatting of your paper, you do not need to position figures and tables at the top and bottom of each column. In fact, all figures, figure captions, and tables can be at the end of the paper. Large figures and tables may span both columns. Place figure captions below the figures; place table titles above the tables. If your figure has two parts, include the labels "(a)" and "(b)" as part of the artwork. Please verify that the figures and tables you mention in the text actually exist. **Please do not include captions as part of the figures. Do not put captions in "text boxes" linked to the figures. Do not put borders around the outside of your figures.** Use the abbreviation "Fig." even at the beginning of a sentence. Do not abbreviate "Table." Tables are numbered with Roman numerals.

Color printing of figures is not available Do not use color unless it is necessary for the proper interpretation of your figures.

Figure axis labels are often a source of confusion. Use words rather than symbols. As an example, write the quantity "Magnetization," or "Magnetization *M*," not just "*M*." Put units in parentheses. Do not label axes only with units. As in Fig. 1, for example, write "Magnetization (A/m)" or "Magnetization ($A \cdot m^{-1}$)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) x 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

B. References

Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

Number footnotes separately in superscripts (Insert | Footnote).[1] Place the actual footnote at the bottom of the column in which it is cited; do not put footnotes in the reference list (endnotes). Use letters for table footnotes (see Table I).

Please note that the references at the end of this document are in the preferred referencing style. Give all authors' names; do not use "*et al*." unless there are six authors or more. Use a space after authors' initials. Papers that have not been published should be cited as "unpublished" [4]. Papers that have been accepted for publication, but not yet specified for an issue should be cited as "to be published" [5]. Papers that have been submitted for publication should be cited as "submitted for publication" [6]. Please give affiliations and addresses for private communications [7].

Capitalize only the first word in a paper title, except for proper nouns and element symbols. For papers published in translation journals, please give the English citation first, followed by the original foreign-language citation [8]. All references **must be** written in Roman alphabet.

C. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have already been defined in the abstract. Abbreviations such as IEEE, SI, ac, and dc do not have to be defined. Abbreviations that incorporate periods should not have spaces: write "C.N.R.S.," not "C. N. R. S." Do not use abbreviations in the title unless they are unavoidable (for example, "IEEE" in the title of this article).

D. Equations

Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Press the tab key and write the equation number in parentheses. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Use parentheses to avoid ambiguities in denominators. Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\,\mathbf{d}\,d\varphi = [\sigma r_2/(2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|z_j - z_i|)\,\lambda^{-1} J_1(\lambda r_2)\,J_0(\lambda r_i)\,d\lambda\,. \tag{1}$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature, but T is the unit tesla). Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ... ."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm x 0.2 cm," not "0.1 x 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) In American English, periods and commas are within quotation marks, like "this period." Other punctuation is "outside"! Avoid contractions; for example, write "do not" instead of "don't." The serial comma is preferred: "A, B, and C" instead of "A, B and C."

If you wish, you may write in the first person singular or plural and use the active voice ("I observed that ..." or "We observed that ..." instead of "It was observed that ..."). Remember to check spelling. If your native language is not English, please get a native English-speaking colleague to carefully proofread your paper.

[1] It is recommended that footnotes be avoided (except for the unnumbered footnote with the receipt date and authors' affiliations on the first page). Instead, try to integrate the footnote information into the text.

VI. Some Common Mistakes

The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

An excellent style manual and source of information for science writers is [9].

VII. Editorial Policy

Each manuscript submitted is subjected to the following review procedure:

- It is reviewed by the editor for general suitability for this publication
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Do not submit a paper you have submitted or published elsewhere. Do not publish "preliminary" data or results. The submitting author is responsible for obtaining agreement of all coauthors and any consent required from sponsors before submitting a paper. It is the obligation of the authors to cite relevant prior work.

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Authors should consider the following points:

1) Technical papers submitted for publication must advance the state of knowledge and must cite relevant prior work.
2) The length of a submitted paper should be commensurate with the importance, or appropriate to the complexity, of the work. For example, an obvious extension of previously published work might not be appropriate for publication or might be adequately treated in just a few pages.
3) Authors must convince both peer reviewers and the editors of the scientific and technical merit of a paper; the standards of proof are higher when extraordinary or unexpected results are reported.
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5) Papers that describe ongoing work or announce the latest technical achievement, which are suitable for presentation at a professional conference, may not be appropriate for publication in "Electronics".

IX. Conclusion

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Appendix

Appendixes, if needed, appear before the acknowledgment.

Acknowledgment

The preferred spelling of the word "acknowledgment" in American English is without an "e" after the "g." Use the singular heading even if you have many acknowledgments. Avoid expressions such as "One of us (S.B.A.) would like to thank ... ." Instead, write "F. A. Author thanks ... ." **Sponsor and financial support acknowledgments are placed in the unnumbered footnote on the first page, not here.**

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