Improving the Gain and Bandwidth of CMOS Circuits with Fe-MgO Tunnel Junctions

Mayank Chakraverty and Valayathoor N. Ramakrishnan

***Abstract*— This paper reports the influence of magnetic tunnel junctions on the electrical response of an operational amplifier (op-amp) circuit. As a baseline, the pure-CMOS operational amplifier has been designed using the 180 nm semiconductor process technology from the Taiwan Semiconductor Manufacturing Company Ltd. and the test bench has been simulated to obtain circuit performance metrics like open loop gain, phase, bandwidth and phase margin. The introduction of a magnetic element can upset the electrical behavior and the same has been observed with the introduction of Fe-MgO tunnel junction on the baseline electrical behavior of the operational amplifier test bench. Possibilities of connecting the tunnel junction to the different nodes of the op-amp test bench have been explored and the consequent drifts in the electrical response have been studied in this paper. Furthermore, an attempt has been made to mirror the transistors in the op-amp circuit with tunnel junctions and the consequent electrical responses have been studied in this paper. Such a magneto-CMOS hybrid circuit configuration can be used for a wide range of novel applications that demand a higher packing density in limited die area.**

***Index Terms*— Ferromagnets, first principles, magnetic elements, MRAMs, tunnel junctions**

Original Research Paper
DOI: 10.53314/ELS2529031C

I. Introduction

Magnetic tunnel junctions (MTJs) are tiny magnetic elements that have a wide range of applications [1]. They are made by depositing two thin films of ferromagnetic material that sandwich another thin film of an oxide or another form of insulator [1-3]. These devices serve as building blocks of magnetoresistive RAMs (MRAMs) where the data is written into the magnetization of the ferromagnetic film and spin dependent tunneling phenomenon governs the conduction mechanism [1, 3, 4]. Being non-volatile, the stored data stays in the magnetization of the tunnel junction as long as the magnetic alignment of the ferromagnetic film is not disturbed by an external field [22], [23]. The stored data is read by the control transistors connected to the tunnel junction [5], [6]. With two ferromagnetic thin films on top and bottom of the insulating oxide layer, this magnetic device can have two resistance states, the low, parallel state resistance (R_p) signifying the relative parallel alignment of magnetic moments of the two ferromagnets and the high, antiparallel state resistance (R_{AP}) signifying an antiparallel alignment of magnetic moments of one ferromagnet in relation to the other [1], [7]-[10]. Resistance switching from low to high state or high to low state is a characteristic property of these devices [1], [11]-[14]. The tunnel junction is usually represented by an equivalent circuit that has a resistor connected to a capacitor in parallel, as reported in [1], [15]-[18].

A tunnel magnetoresistance ratio (TMR) is typically defined, in terms of the junction resistances in the parallel and antiparallel magnetized states (R_p and R_{AP}, respectively) [1], to quantify the percentage change in the junction resistance. This is expressed in equation (1).

$$TMR = \frac{\Delta R}{R_{AP}} \times 100\% = \frac{R_{AP}-R_P}{R_{AP}} \times 100\% \quad (1)$$

The values of R_p and R_{AP} have been computed from the I-V characteristics of the Fe-MgO MTJ through First Principles Local Spin Density Approxiation (LSDA) bandstructure calculations. The geometry of the device employed for the bandstructure calculations has been used to estimate the MTJ capacitance value. The Fe-MgO MTJ employed for device level LSDA bandstructure calculations reports R_p to be 1279 Ohms while the value of R_{AP} is found to be 13.8 Mega Ohms [1]. These resistance and capacitance values have been used in the equivalent circuit comprised of a resistor and a capacitor, as derived in [1], that replicates the behavior of the MTJ in circuit simulations.

Based on such band structure calculations and the device geometry, the resistance (R_p and R_{AP}) and capacitance values for simulating a Fe-MgO tunnel junction in the form of an equivalent circuit have been derived [1], [19] and the same values have been used in this paper. In addition to integrating such tunnel junctions in MRAMs, the prospect of incorporating these tiny magnetic devices in CMOS based circuits and studying the impact of these nanoscale magnetic devices on the electrical response of the circuits has been a topic of interest [20], [21]. In this paper, the very popular operational amplifier circuit [24]

Manuscript received on January 31st, 2024. Received in revised form on September 2nd and November 29th, 2024. Accepted for publication on December 2nd, 2024.

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has been chosen for such a study. Often known by the name op-amp, the operational amplifier is a device that is primarily used for voltage amplification [25], [26]. The design is such that, in between the output and input terminals, resistors and capacitors serve as external feedback components that are connected to the voltage-amplifying device [27]. By virtue of the many feedback topologies, whether resistive, capacitive, or both, the amplifier can perform a variety of different operations, hence the name "Operational Amplifier" [28]. The resulting function or operation of the amplifying device is decided by these feedback components. Parameters like open loop gain, phase, bandwidth and phase margin are critical to determining the electrical response of an op-amp circuit [29] and hence the op-amp test bench has been simulated to obtain the open loop gain, phase, bandwidth and phase margin, without the tunnel junction and then with the inclusion of the Fe-MgO tunnel junction.

II. Operational Amplifier Basics

An integrated circuit with the ability to amplify weak electric impulses is called an operational amplifier [30]. In general, there are two input pins and one output pin on an operational amplifier. Its primary function is to output the voltage difference between the two input pins after being amplified [30]-[32].

A linear integrated circuit (IC) with numerous terminals is all that is needed to create an operational amplifier [33]. Op-amps are voltage amplifiers that are intended to be used in conjunction with external feedback devices, such as resistors and capacitors, placed between the input and output terminals of the device. It is a high-gain electrical voltage amplifier that typically produces a single-ended output from a differential input. Because they are utilized in so many different consumer, industrial, and scientific applications, opto-amplifiers are among the most commonly used electronic devices in use today.

Op amps typically feature three terminals: an output port with low impedance and two high-impedance input ports. The non-inverting input is represented by a positive (+) sign, whereas the inverting input is indicated by a minus (-) sign. Operational amplifiers are helpful for a range of analog operations such as power, control, and signal chain applications. They function by amplifying the voltage differential between the inputs. The positive and negative terminals of a DC voltage source are connected to the V+ and V− power supply terminals, respectively. If the V+ and V− common terminals are not connected to a ground or reference point, the op-amp could be damaged by twice the supply voltage.

Op amps are associated with numerous significant features and aspects (refer to Fig. 1). A more thorough description of these traits can be found below.

The operational amplifier's gain attained without any feedback being applied to the circuit is known as the open-loop gain (designated as "A" in Fig. 1). This indicates that the loop, or feedback path, is open. With the exception of voltage comparators, an open-loop gain frequently needs to be extremely large (10,000+) in order to be useful on its own [34]. Input terminal voltages are compared by voltage comparators. Voltage comparators can drive the output to either the positive or negative rails even with tiny voltage differentials [35]. In closed-loop configurations, high open-loop gains are advantageous because they allow stable circuit behaviors across variations in process, temperature, and signal.

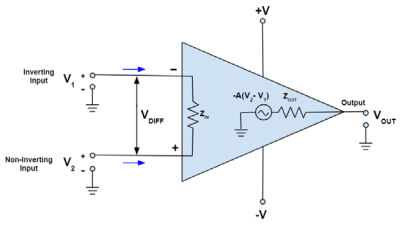


Fig. 1 Operational amplifier schematic

An ideal operational amplifier (op amp) would be able to maintain a high gain at any signal frequency and have an infinite bandwidth (BW). Nonetheless, every operational amplifier possesses a limited bandwidth, commonly referred to as the "-3dB point," at which the gain starts to decrease with an increase in frequency. The amplifier's gain then drops at a rate of -20dB/decade as the frequency rises. Higher BW op amps perform better because they can sustain higher gains at higher frequencies; however, this higher gain comes at the expense of higher power consumption or higher cost [36], [37].

Gain bandwidth product (GBP): GBP is a function of the gain and bandwidth of the amplifier, as the name implies [38]. Equation (2) can be used to calculate GBP, which is a constant value across the curve.

$$\text{GBP} = \text{Gain} \times \text{Bandwidth} = A \times BW \tag{2}$$

The frequency point at which the gain of the operational amplifier approaches unity is used to measure GBP. This is helpful because it lets the user figure out how much gain the device has open-loop at various frequencies. The GBP of an operational amplifier is typically a measure of its usefulness and performance because higher GBP op amps can be used to achieve higher frequencies with better performance [39].

Depending on the application and performance requirements, there are numerous other factors that could affect your design in addition to these primary ones when choosing an operational amplifier for any application. Supply voltages, noise, quiescent current, and input offset voltage are additional typical parameters [40].

Using an operational amplifier has a lot of benefits. Operational amplifiers are typically integrated circuits (ICs), are widely accessible, and have an endless range of selectable performance levels to suit the requirements of any application. Op amps are a vital component of many analog applications, such as comparator circuits, voltage buffers, filter designs, and many more, due to their wide range of applications [41]. Furthermore, before developing actual designs, most companies offer simulation support to designers, such as PSPICE models, to validate their operational amplifier designs. The fact that operational amplifiers are analog circuits and necessitate an understanding

of analog fundamentals like loading, frequency response, and stability are some of their drawbacks. Designing an op amp circuit that looks straightforward only to discover upon turning it on that it oscillates is a frequent occurrence. The designer usually needs to have moderate to high experience with analog design because of some of the important parameters that were previously discussed, and they need to understand how those parameters affect their design.

III. Related Works

Ever since the magnetic tunnel junctions have been found to be closely compatible with the current silicon-based manufacturing line, a lot of interests have spiked on integrating such magnetic elements into conventional CMOS circuits.

Simulation and fabrication of such magneto-CMOS hybrid circuits have widely been researched upon. In order to simulate such hybrid MTJ/CMOS circuits, G. Panagopoulos et. al [42] have introduced a SPICE-based framework. For hybrid MTJ/CMOS circuits developed entirely in SPICE, they have proposed a physics-based simulation framework that makes use of solely built-in components, like capacitors and voltage/current dependent voltage/current sources. Accuracy, quick simulation time, compatibility with current MOSFET SPICE models, simplicity of use, and ease of implementation are some advantages of this model. By enabling the exploration of performance tuning knobs at multiple levels of abstraction, from materials to the circuit level, the suggested framework closes the gap between materials, devices, and circuits. MTJ modeling in the proposed simulation framework incorporates spin-torque and an external magnetic field or fields and is based on the Landau-Lifshitz-Gilbert (LLG) equation. LLG is implemented using SPICE-integrated voltage-dependent current sources and capacitors, in addition to the heat diffusion equation, thermal variations, and electron transport. Because user-defined parameters govern the device dimensions, including MgO thickness and area, the suggested simulation framework is configurable. This model has been shown to correlate well with experimental data.

Using resistor-based temperature sensors (-55°C ∼ 125°C) and sigma-delta analog-to-digital converters (SD-ADC) as two case studies where high resistance is required and limits scaling down, the work done by Y.-a Wu et. al [43] exploits tunnel magnetoresistance-based replacement in reducing layout penalty of on-chip passive component during circuit design. Two temperature adaptive write schemes for MRAM are also suggested as additional uses for the suggested MTJ-based temperature sensor, considering the application in MRAM, the mainstream field of MTJ process, and addressing the issues of MRAM in wide temperature write operation. Major attributes associated with MTJ as the passive component, such as area, variation, and temperature characteristics, are covered in the study of these circuits. MTJ-based resistors are used in place of large CMOS resistance in SD-ADC and bridge transducer in resistor-based temperature sensors. Based on the simulation results, the resistor-capacitor (RC) integrator's passive resistor layout area was significantly decreased by 94.52% when compared to a completely 28nm CMOS design, or 94.13% for wide temperature application, while maintaining nearly the same performance. Furthermore, as compared to standard CMOS resistor-based temperature sensor designs, the MTJ-based bridge transducer in resistor-based temperature sensors can reduce the resistance layout area by more than 90% with improved linearity. The two distinct adaptive write circuits, which are based on the MTJ-based temperature sensor, aid in lowering the write power consumption and MRAM delay for wide temperature use, respectively. Furthermore, because MTJs are programmable, one can program their states to make the hybrid resistor's resistance changeable and controlled, giving it an advantage over a pure passive resistor. Therefore, it is possible to create a multimode circuit with switchable performance.

Adiabatic designs and logic-in-memory (LiM) structures that employ magnetic devices are two effective ways to achieve low power designs. This has been demonstrated by F. Sharifi et al. [44], by designing one-bit full adder circuits, AND/NAND, and XOR/XNOR circuits using a new adiabatic hybrid MTJ/CMOS structure. Synopsys HSPICE with 32nm CMOS technology has been used to model the designs, and they have been contrasted with non-adiabatic hybrid MTJ/CMOS circuits. Comparing the proposed XOR, AND, and full adder to the state of the art MTJ/CMOS full adder configurations, their respective power consumptions have been found to be nearly 13, 6, and 7 times lower.

IV. Baseline Simulation

To carry out the baseline simulation, an op-amp circuit has been designed using devices from the 180 nm semiconductor process technology from the Taiwan Semiconductor Manufacturing Company Ltd. (TSMC). A technology node in semiconductor manufacturing refers to the minimum feature size or critical dimension that can be produced on a semiconductor chip. It is typically measured in nanometers (nm) and represents the scale at which transistors and other components are fabricated on an integrated circuit. The technology node is a key parameter that determines the performance, power efficiency, and density of a semiconductor device. As technology nodes become smaller, more transistors can be packed onto a single chip, enabling increased processing power, faster speeds, and lower power consumption. Cadence Virtuoso schematic editor has been used to design the circuit and simulations have been carried out in Analog Design Environment (ADE-XL) using the SPICE models from TSMC. An important reason for selecting the 180 nm process node from TSMC is the stability of the process, proven record of better analog integration at 180 nm. Also, with 180 nm process, there is a possibility of obtaining higher sampling rates at lower power with smaller die sizes.

The schematic of the designed op-amp circuit is depicted in Fig. 2. The design parameter details have been summarized in Table I. The next step is to generate a symbol for the op-amp. Once the op-amp circuit has been fully rendered in its schematic form, the next essential step is to simulate it, to verify that it fulfills the specifications. The first step in testing a design is cre-

ating one or more test benches. A test bench is a schematic that includes the top-level schematic as a module and provides it with stimuli. The outputs of the design in response to the stimuli can be observed during simulation. To simulate the op-amp circuit depicted in Fig. 2, such a test bench has been built. This is depicted in Fig. 3.

TABLE I
DESIGN PARAMETERS OF BASELINE OP-AMP CIRCUIT

Inst	Parameters		Inst	Parameters
MP0	wt = 10um		**MP1**	wt = 10um
	l = 1um			l° = 5um
	ng = 1			ng = 1
MN0	wt = 25um		**MN1**	wt = 25um
	l = 3um			l = 3um
	ng = 2			ng = 2
	m = 2			m = 2
MN2	wt = 5um		**MN3**	wt = 5um
	l = 3um			l = 3um
	ng = 1			ng = 1
MN4	wt = 125um		**MP2**	wt = 210um
	l = 3um			l = 3um
	ng = 4			ng = 4
R0	R = 34.70kOhm		**C0**	C = 1,792pF
	l = 212um			w = 30um
	w = 2um			l = 30um
	s = 5			m = 4

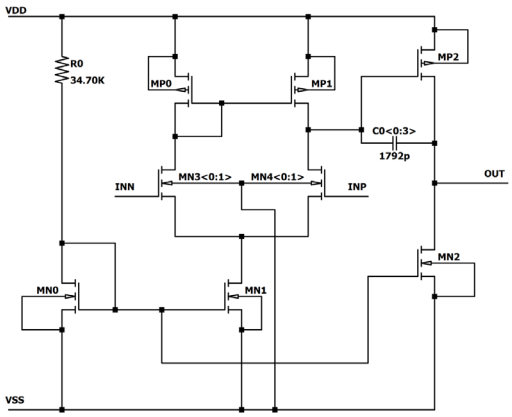


Fig. 2 Schematic of an op-amp circuit

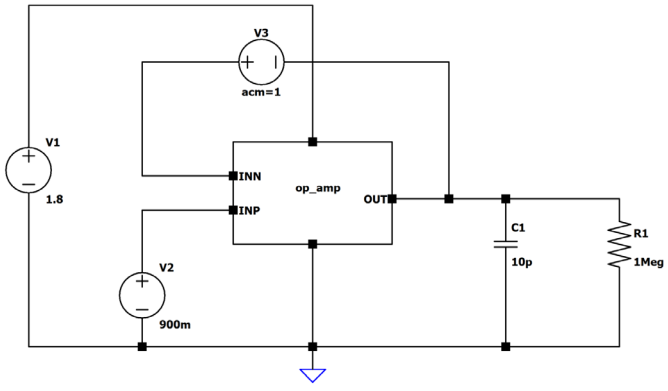


Fig. 3 Op-amp test bench (Baseline)

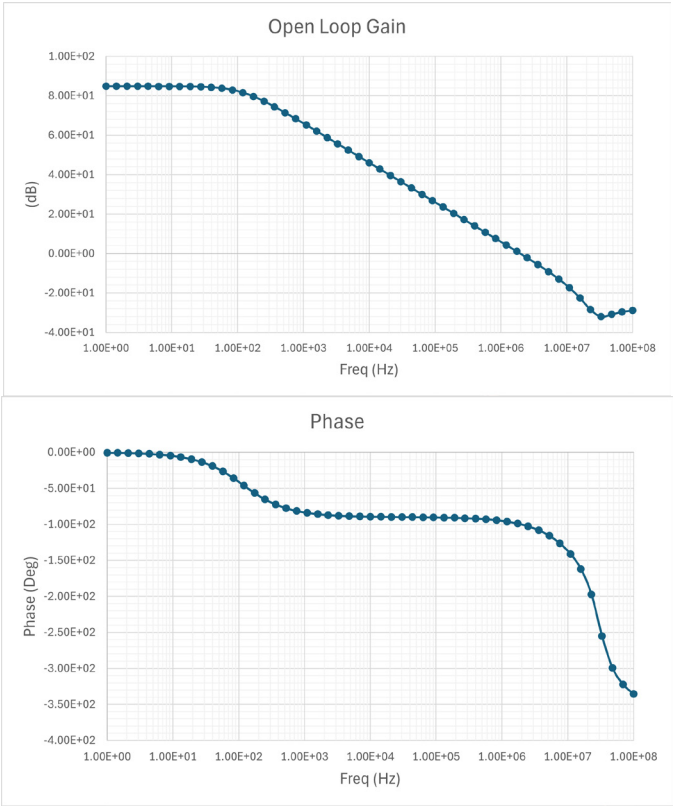


Fig. 4 Open loop gain and phase response from baseline op-amp simulation

The operational amplifier has been used in closed loop configuration and a test sinusoidal voltage source is inserted, setting AC Magnitude = 2.5V, Frequency = 10 kHz, connecting it to the input terminal INP. The VDD is set to 1.98V. The open loop gain and the phase response obtained from the simulated op-amp test bench of Fig. 3 is depicted in Fig. 4. In addition, the bandwidth and phase margin thus obtained are 127.7 Hertz and 79.81 degrees respectively.

V. INCORPORATING MTJS IN OP-AMP TEST BENCH

There can be several possible ways of connecting the magnetic element to the op-amp configuration. In this section of the paper, the focus has been on connecting the tunnel junction to the op-amp test bench circuit in a variety of ways and observing the drift in the circuit parameters and the electrical response. The aim of this work is to study the impact of such magnetic elements on the electrical behavior of pure-CMOS circuits like the operational amplifier but this can be termed a hypothetical approach, as there is no predefined application space that the hybrid circuit configuration can cater to. However, there are possibilities of applications of such magneto-CMOS hybrid circuits based on their electrical response. Such CMOS circuits with integrated Fe-MgO tunnel junctions could be applied in the industry for developing high-density, high-performance electronic components, such as advanced memory devices, sensors, and signal processing circuits. These hybrid circuits can offer enhanced gain, bandwidth, and reduced die area, making

them suitable for applications in telecommunications, data storage, and compact consumer electronics.

The first set of simulations has been carried out by connecting the tunnel junction to the INN node of the op-amp symbol. This is depicted in Fig. 5. Throughout this paper, the MTJ is depicted by connecting R_p (=1279 Ohms) in parallel with the MTJ capacitor, C. The R_{AP}, as reported in [1], is very high (13.8 Mega Ohms) and it has been observed that implementing the MTJ with R_{AP} and MTJ capacitor does not really impact the electrical response of the circuit under test. The corresponding bandwidth and phase margin have been computed, as tabulated in Table II, and the resulting open loop gain and phase response have been plotted, as depicted graphically in Fig. 10 and Fig. 11, respectively.

TABLE II
BANDWIDTH AND PHASE MARGIN OF MTJ BASED OP-AMP TEST BENCH

CIRCUIT TOPOLOGY	BANDWIDTH (HZ)	PHASE MARGIN (DEG.)
BASELINE	127.7	79.81
TOPOLOGY 1	584.1K	79.81
TOPOLOGY 2	584.1K	79.81
TOPOLOGY 3	584.1K	79.81
TOPOLOGY 4	659.7K	104.7
TOPOLOGY 5	673.4K	86.07

In the next variant of the circuit topology, the tunnel junction has been connected to the INP node of the op-amp symbol, as shown in Fig. 6, and the corresponding open loop gain and phase response are plotted in Fig. 10 and Fig. 11. The bandwidth and phase margin values thus computed can be found in Table II.

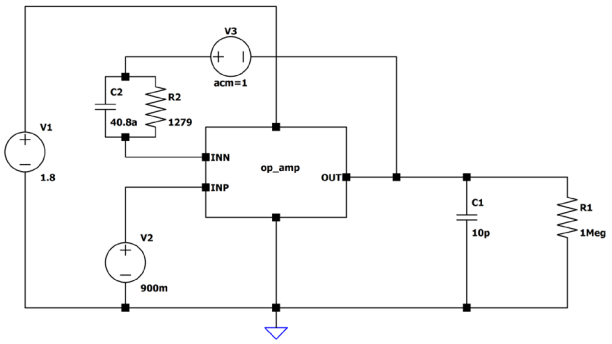


Fig. 5. Op-amp test bench with MTJ connected to INN (Topology 1)

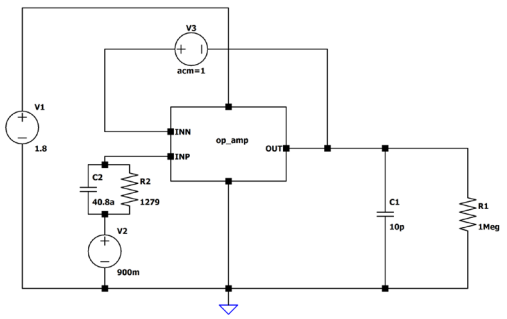


Fig. 6 Op-amp test bench with MTJ connected to INP (Topology 2)

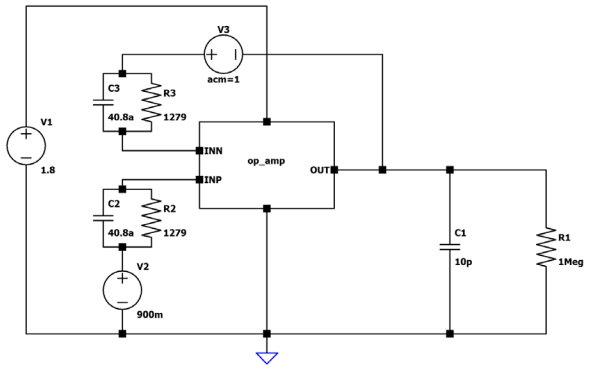


Fig. 7 Op-amp test bench with MTJs connected to INN and INP (Topology 3)

Unlike the two previous cases where the op-amp test bench has been simulated with a single tunnel junction, the next magneto-CMOS circuit topology has a tunnel junction connected to each of the two input nodes (INN, INP) of the op-amp symbol; the circuit is shown in Fig. 7. With two tunnel junctions in the design, the silicon area does not go up as the tunnel junctions are nanoscale, extremely tiny devices relative to the other components in the circuit. The open loop gain and phase response have been plotted in Fig. 10 and Fig. 11, respectively, and the bandwidth and phase margin have been computed as well, as presented in Table II.

Another couple of possibilities of a hybrid magneto-CMOS circuit can be with the tunnel junction connected to the OUT node of the op-amp symbol, and with the tunnel junction connected to the power (VDD) line of the test bench. This is depicted in Fig. 8 and Fig. 9, respectively.

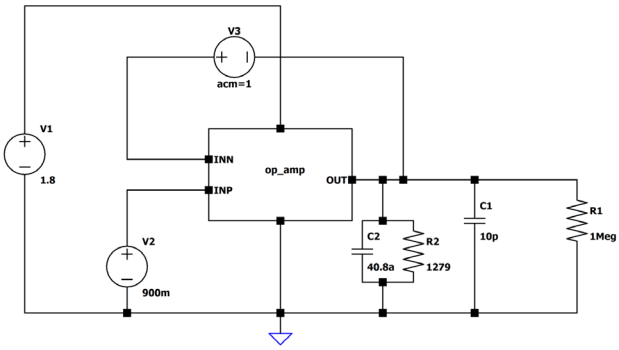


Fig. 8 Op-amp test bench with MTJ connected to OUT (Topology 4)

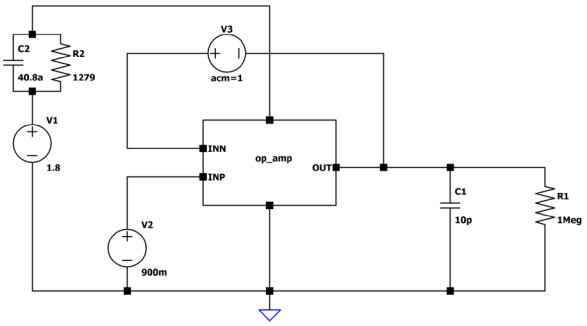


Fig. 9 Op-amp test bench with MTJ connected to VDD (Topology 5)

The primary purpose of an op-amp is to increase the input signal, and the functionality of the op-amp improves with an increase in the open loop gain. Open loop gain is defined as gain when there is no positive feedback nor negative input. Based on the simulation results obtained so far, connecting the op-amp to the tunnel junction in the manner that is depicted in topology 4 and topology 5 result in lower open loop gain, in comparison with the results obtained using topologies 1, 2 and 3.

Higher frequency signals can be amplified by the op-amp with a larger bandwidth, which results in faster speeds. The bandwidth of the op amp, in the electrical world, is the frequency at which the signal gain is 1/sqrt(2), or 0.707 of the ideal value. Op-amps can function with expected behavior up to this maximum frequency. It can be seen from Table II that the bandwidth and phase margin values obtained from the baseline test bench simulation are low as compared to the values obtained from simulation of op-amp test benches with tunnel junctions connected to either or both the inputs, at the output or even to VDD. In fact, there is a marked increase in the bandwidth as soon as the magnetic element is introduced into the pure-CMOS circuit. From this observation, a designer can conclude on using tunnel junctions in such CMOS circuits as op-amps to enhance the bandwidth and phase margin at the expense of extremely low die area overhead and this has a cost advantage as well.

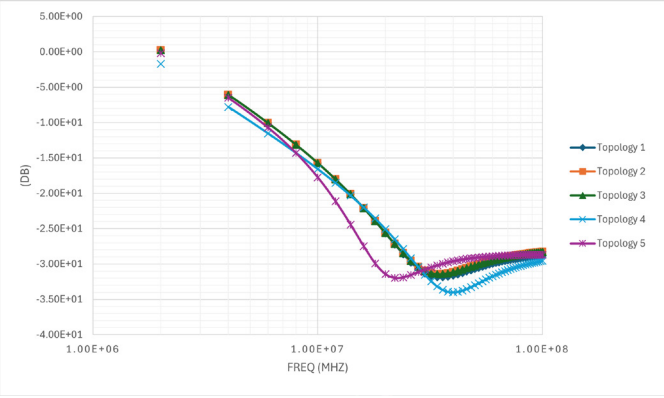


Fig. 10 Open loop gain of op-amp test bench with tunnel junctions

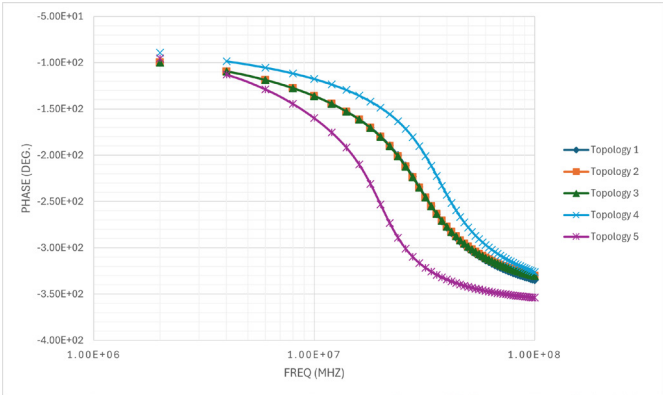


Fig. 11 Phase response of op-amp test bench with tunnel junctions

When the gain of the amplifier crosses 0dB, phase margin measures the degree of phase shift. Essentially, it serves as a gauge for how likely the system's second pole is to lead to instability. About a decade before the corner frequency, phase changes begin. Less than 180° of phase shift is required. The amplifier's real phase shift, measured in degrees, is the phase margin, which is 180°. Usually, anything above 45° is acceptable. System stability increases with phase margin. Reduced phase margin results from capacitive loading. In the simulation results reported so far, the topology 4 results in the highest phase margin followed by topology 5 while the remaining three topologies report a relatively lower phase margin.

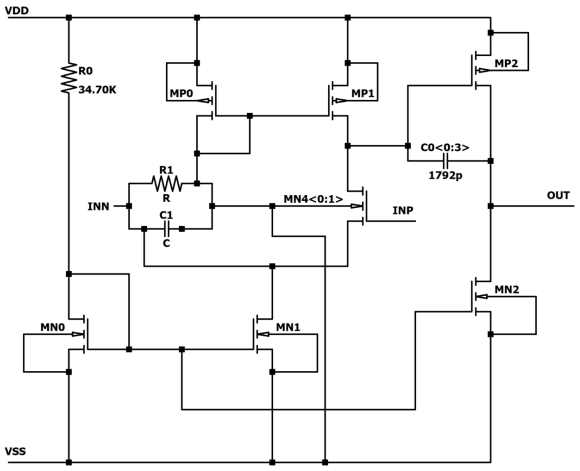
VI. MTJ Based Op-Amp Circuit Simulation

In this section of the paper, an attempt has been made to replace the transistors in differential pair used in the op-amp circuit depicted in Fig. 2 with the Fe-MgO tunnel junction and study the impact on the electrical behavior of the op-amp test bench. So, all the changes in the design have been done within the symbol hierarchy of the circuit and the baseline test bench of Fig. 3 has not been altered for simulation in this part of the work.

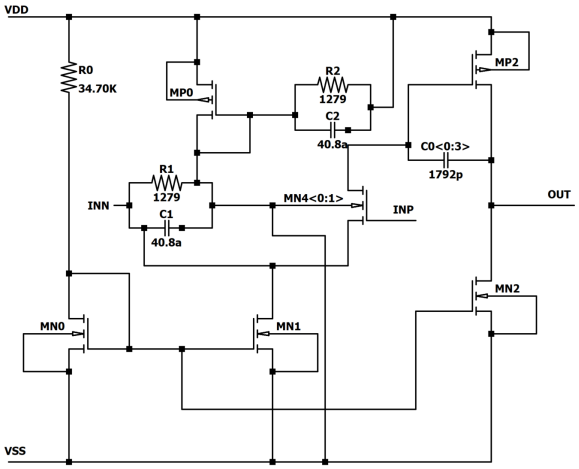
Replacing the transistors in the differential pair, one by one, has resulted in four op-amp circuit variations that have been simulated in this paper. This is depicted in Fig. 12 (a) – (d). A definite pattern has been followed while replacing the MOSFETs with tunnel junctions. For instance, the lower left NMOS transistor of the differential pair is the first device to be replaced by the Fe-MgO tunnel junction, followed by the estimation of bandwidth and phase margin along with simulating the open loop configuration of the corresponding test bench, thus obtaining the gain and phase as done in the previous section of the paper. As compared to the baseline simulation, i.e., with no tunnel junction involved in the op-amp configuration, the bandwidth and phase margin thus obtained are high. This behavior is again consistent with the results reported in the previous section of the paper, where the inclusion of a tunnel junction helped raising the bandwidth of the simulated circuit. Next, the diagonal PMOS device has been replaced by the magnetic element and the performance metrics have been obtained. In the third iteration, the other PMOS device in the differential pair has been replaced, followed by replacement of the only remaining NMOS transistor in the differential pair. The bandwidth and phase margin obtained from simulating each of the circuit iterations have been presented in Table III. While, the open loop gain and phase response of each circuit variation have been plotted in Fig. 13 and Fig. 14, respectively.

Another observation from the simulation results is that the highest bandwidth is reported by the op-amp circuit where all the transistors in the differential pair have been replaced by tunnel junctions. This highlights the role of tunnel junctions in raising the bandwidth of CMOS circuits with magnetic tunnel junctions as part of it. The corresponding phase margin is also high. The same circuit also reports the highest open loop gain, resulting in the highest gain-bandwidth product among all the circuits that have been simulated in this paper. The results in Table III are quite consistent with plots in Fig. 13 and Fig. 14 as the circuits with tunnel junction replacing the diagonal tran-

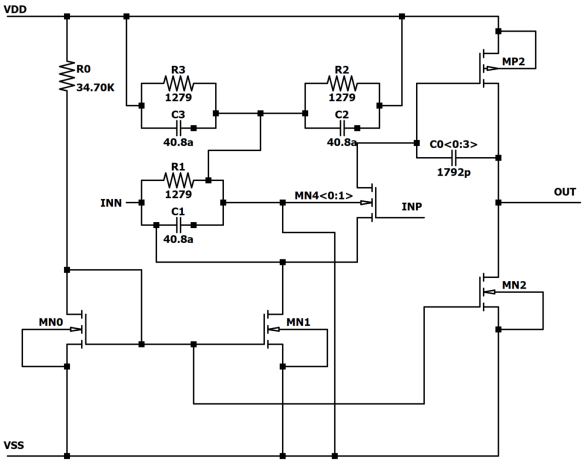
sistors, one by one, in the differential pair result in the same bandwidth and phase margin. From Fig. 13 and Fig. 14, it is seen that the same two circuits result in overlapping open loop gain and phase response.



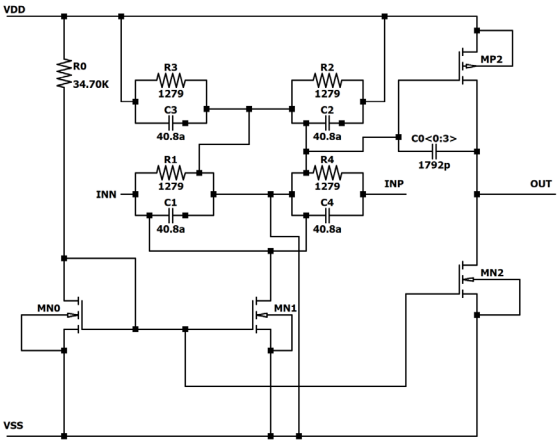
(a)



(b)



(c)



(d)

Fig. 12 Schematics of op-amp circuit with MTJs replacing NMOS and PMOS devices in differential pair

TABLE III
BANDWIDTH AND PHASE MARGIN OF MTJ BASED OP-AMP TEST CIRCUIT

OP-AMP VARIATION	BANDWIDTH (HZ)	PHASE MARGIN (DEG.)
NO VARIATION (BASELINE)	127.7	79.81
OP-AMP VARIATION 1	606.3K	93.19
OP-AMP VARIATION 2	588.4K	176.2
OP-AMP VARIATION 3	588.4K	176.2
OP-AMP VARIATION 4	657.5K	113.4

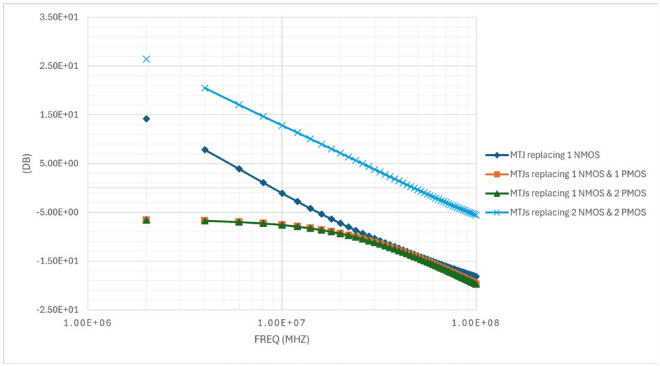


Fig. 13 Open loop gain of op-amp circuit with MTJs replacing NMOS and PMOS devices in differential pair

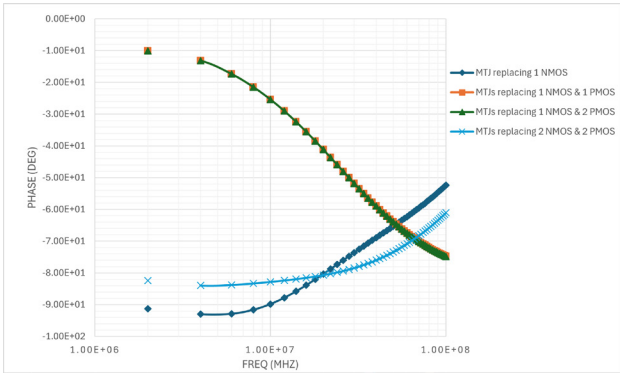


Fig. 14 Phase response of op-amp circuit with MTJs replacing NMOS and PMOS devices in differential pair

VII. Conclusions And Future Work

This paper has presented interesting results obtained from the simulation of a tunnel junction based operational amplifier. Two sets of simulations have been carried out. In the first set, the effect of adding a tunnel junction to the op-amp test bench has been studied and the electrical behavior has been compared with the simulation results of baseline op-amp test bench. In the next set, the transistors have been replaced by tunnel junctions, one at a time, followed by simulation of the resulting op-amp circuit. In both the sets of simulation, it is observed that the introduction of tunnel junction increases the bandwidth and the phase margin of the circuit, the open loop gain also improves with the addition of tunnel junction as compared to the baseline op-amp simulation. The results from the magneto-CMOS op-amp circuit simulation open up such hybrid circuits for many applications that require high gain bandwidth product while consuming very little die area as the tunnel junctions with nanoscale device dimensions do not add to area overhead but do influence the electrical behavior of pure CMOS circuits in a positive direction.

The plan is to take this work forward to the next stage and attempt to fabricate such a magneto-CMOS circuit on silicon and characterize the circuit to obtain real electrical response of the hybrid circuit based on measured silicon data.

Acknowledgments

We would like to thank VIT University, Vellore, India, for supporting this research work. We would also like to thank Dr. Vipin Madangarli, Director, RF Analog and Mixed Signal Design Enablement, GLOBALFOUNDRIES (Bangalore, India) for his encouragement and support.

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