An Approach to Design a Low Power High-Speed Full Adder Circuit Based on Logical Effort

S. Goswami, V. Chandana, and A. Dandapat

***Abstract*—The logical effort method is a technique for accurately estimating the delay of a CMOS circuit. This method is computed as a ratio of capacitances. In this work we propose a low-power full adder circuit and compare it with three established low power full adder circuits. The circuits were designed utilizing Cadence Virtuoso software and GPDK 45nm technology. A comparison was conducted based on delay, average power, power delay product, and transistor count. In this work, all circuits are resized to achieve minimum delay according to the logical effort. It has been shown that the proposed design (design 4) is showing better performance in terms of average power, delay of sum and delay of carry than other designs by 34.23%, 26.81%, and 4.33%, respectively.**

***Index Terms*—CMOS logic, Full adder, GPDK45, Logical effort, Low power.**

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I. Introduction

THE field of logical effort calculation plays a pivotal role in the design and optimization of CMOS logic gates. The logical effort of a gate is a critical metric that determines the relative performance of different gate configurations. In this context, it is essential to build upon the established methodologies and insights garnered from prior research [1], [2]. Designers are aiming to create full adders with as few transistors as feasible to get the best power consumption, delay, and area. Many full adders with different logic types were published [3]–[6]. Chip designers must decide on the appropriate circuit layout, transistor size, and logic stage count to minimize delay in digital circuits. Logical effort addresses all these concerns. The aforementioned is the proportion of capacitances at the gate that generate an equivalent current to that of an inverter [7].

A. Logic Gate Delay

The logical effort of a circuit can be defined by the following equations.

$$d = \frac{dabs}{\tau} \tag{1}$$

where $dabs$ denotes the absolute delay and $\tau = 3RC$. Delay comes with two components

$$d = f + p \tag{2}$$

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Effort delay is $f = gh$ (also known as stage effort), so that the delay is expressed as

$$d = gh + p \tag{3}$$

where:

- g is logical effort, which measures relative ability of a gate to deliver current,
- h is electrical effort, which represents output to input capacitance ratio (sometimes termed as fan-out) [7], [8]

$$h = \frac{Cout}{Cin}, \tag{4}$$

- p is parasitic delay, which represents delay of a gate driving no load (it is set by internal parasitic capacitance).

The definitions of all terms in logical effort are stated in Table I.

B. Logical Effort Calculation

Several seminal works, including references [7] and [11], have laid the groundwork for logical effort calculations. These contributions have elucidated the intricate relationship between gate characteristics, such as capacitance ratios, and the resulting logical effort. Moreover, the fundamental equation, $C_g = L \cdot W \cdot C_{ox}$, establishes a crucial link between capacitance, oxide capacitance, and width, further underlining the significance of width adjustments in logical effort optimization.

In the realm of CMOS processes, the choice of transistors, with NMOS and PMOS serving as pull-down and pull-up transistors, respectively, is a well-established convention. This practice is underpinned by the inherent disparities in carrier mobility, with electrons dominating in NMOS and holes in PMOS. The implications of these distinctions are encapsulated

TABLE I
Definitions Of All Terms In Logical Effort [7]

Term	Stage	Path
Number of Stage	1	N
Logical-Effort	g	$G = \pi g_i$
Electrical-Effort	$h = \frac{C_{out}}{C_{in}}$	$H = \frac{C_{outpath}}{C_{inpath}}$
Branching-Effort	$b = C_{onpath}$ $+C_{offpath}/C_{onpath}$	$B = \pi b_i$
Effort [7] [9]	$f = gh$	$F = GBH$
Effort-Delay	f	$D_F = \sum g_i h_i$
Parasitic-Delay	p	$P = \sum p_i$
Delay [10]	$d = f + p = gh + p$	$D = \sum d_i = D_F + P$

in the current equations (5) and (6), governing the behavior of MOSFETs in their linear operating zones.

Thus, NMOS mobility μ_n is greater than PMOS mobility μ_p. In the linear zone, for N-channel MOSFET the current equation is

$$I_{DS} = \mu_n \cdot C_{ox} \cdot \frac{W_n}{L_n} \cdot [(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2}] \quad (5)$$

For a P-channel MOSFET operating in the linear region, the governing equation is

$$I_{SD} = \mu_p \cdot C_{ox} \cdot \frac{W_p}{L_p} \cdot [(V_{GS} - V_T) \cdot V_{SD} - \frac{V_{SD}^2}{2}] \quad (6)$$

When comparing PMOS with NMOS, we often assume the same voltage and constant current source. Thus, if equations (5) and (6) of the current formulas are equivalent, C_{ox} and voltages that are common on both sides are eliminated. After canceling, we get the equation

$$\mu_p \cdot \frac{W_p}{L_p} = \mu_n \cdot \frac{W_n}{L_n} \quad (7)$$

Keeping the length in (7) constant is a necessary condition for any practical circuit. This yields

$$W_p = W_n \cdot \frac{\mu_n}{\mu_p} \quad (8)$$

W_p is bigger than W_n because the mobility of n-type electrons is higher than the mobility of p-type holes. PMOS is, therefore, always larger than NMOS.

The inverter, which is shown in Fig. 1(a), contains a 2W wide pull-up transistor and a pull-down transistor whose width is W, since PMOS is wider than NMOS. Therefore, the total input capacitance will be $W + 2W = 3W$. Logical effort of the inverter is $3W/3W = 1$. The pull-down transistors for the NAND gate in Fig. 1(b) are connected in series, giving each transistor a conductance that is double that of the pull-down transistor for the reference inverter. In order to achieve the same pull-down drive as the pull-up transistor inverter, the pull-up transistors would need to be as wide as the inverter. The aggregate input capacitance of each input signal is equivalent to the summation of the widths of the pull-down and pull-up transistor, i.e., $C_i = 2 + 2 = 4$. $C_{inv} = 1 + 2 = 3$ is the input capacitance of the inverter with equal output drive. The logical effort per input of the 2-input NAND gate is, thus, $g = \frac{4}{3}$.

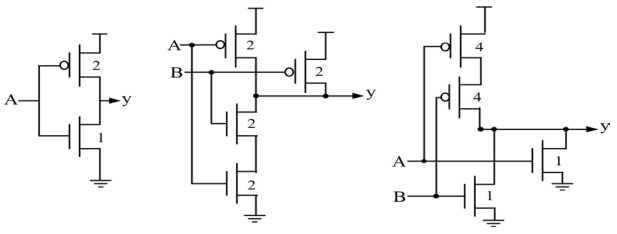

Fig. 1. Logic gates: (a) inverter, (b) two-input NAND, and (c) two-input NOR gate [2], [5].

Fig. 1(c) depicts the NOR gate in a comparable manner. In order to attain an equivalent pull-down drive to that of the inverter, the pull-down transistors must have a width of one unit. It is necessary to have four units between the pull-up transistors in a series configuration to achieve an equivalent pull-up drive as that of the inverter transistors. We can calculate the logical effort of the NOR gate as $g = \frac{5}{3}$ by adding up the input capacitance.

In the process of logic gate design, CMOS transistors are represented as ideal resistors in order to produce an output drive that is equivalent to that of the *Reference Inverter*. In the absence of transistor activation, the resistor exhibits zero conductance. However, when the transistor is activated, the conductance of the resistor is commensurate with its width. The evaluation of transistor conductance involves the amalgamation of the conductance of the transistor network, utilizing established principles for measuring the conductance of a resistor network that comprises parallel as well as series connections to the resistor. Whilst this model may be a rough estimation, it effectively characterizes the efficiency of gate logic, thereby, enabling the construction of expeditious structures.

The three low-power full adder circuits previously disclosed are compared to the new low-power single-bit full adder proposed in this paper [5]–[13]. The circuits are simulated using the Cadence Virtuoso tool and GPDK 45nm technology, and their performance is evaluated based on average power, delay, power delay product, and transistor count. The remaining sections are organized as follows.

In Section II, the design of a low-power full adder circuit and the computation of logical effort are presented. Simulations to determine logical effort and its calculation from a graph are shown in Section III. Section IV contains the results discussion. Finally, Section V presents the conclusion in its final position.

II. Design Of A Low-Power Full Adder And Calculation Of Logical Effort

A low-power full adder circuit is proposed and compared with the three published circuits. The proposed low power full adder circuit shown in Design-4 and the three published circuits are shown in Design-1, 2, and 3, which are from [5] to [14], respectively, and the logical effort values are given for the designs. Design-1 [5], which is shown in Fig. 2, is a hybrid full adder circuit designed by combining CMOS and pass-transistor logic styles. This design is divided into three modules: XOR, inverter, and multiplexer. The XOR module (based on pass transistor logic) generates intermediate signal $A \oplus B$ that is fed to an inverter, which gives $A \odot B$. These signals are afterwards used as selection lines in the multiplexer module [15], [6] (based on pass-transistor logic style) that includes two transmission gate based multiplexers to generate sum and carry. The logical effort in Fig. 2 has four stages, i.e., inverter (used for inputs A and B) for which we know $g = 1$, XOR which gives $g = \frac{2+1+2+1}{3} = 2$, inverter (used to get XNOR output) with $g = 1$, and multiplexer with $g = 2$ for both sum and carry, so that the g value will be the same.

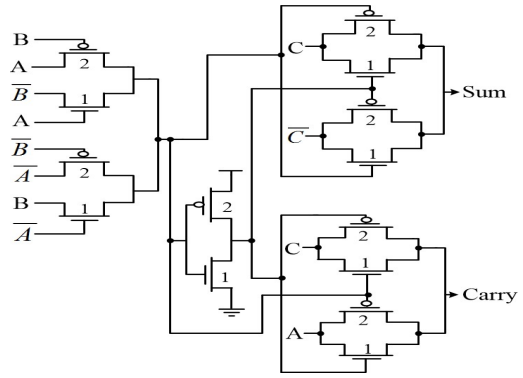

Fig. 2. Low-Power Hybrid Full Adder (Design-1 [5]).

From Fig. 2, it is clear that we need to multiply the values of logical effort for all four stages to get the final g value for sum and carry:

- Sum: $g = 1 \cdot 2 \cdot 1 \cdot 2 = 4$
- Carry: $g = 1 \cdot 2 \cdot 1 \cdot 2 = 4$

Design-2 [14], which is shown in Fig. 3, uses a modified XNOR circuit where the power consumption is reduced significantly by deliberate use of weak inverter and the same XNOR circuit is again used to produce sum. Then, a multiplexer with select lines of XOR and XNOR is used to produce carry. The circuit on Fig. 3 has 4 stages for both sum and carry, but for sum it has inverter (used for input B) with $g = 1$, XOR which gives $g = \frac{2+1+2+1}{3} = 2$, inverter (used to get XNOR output) with $g = 1$, and XOR (for generating sum), which gives $g = \frac{2+1+2+1}{3} = 2$. For carry, it has inverter (used for input B) for which we know that $g = 1$, XOR which gives $g = \frac{2+1+2+1}{3} = 2$, inverter (used to get XNOR output) with $g = 1$, and multiplexer with $g = 2$. Therefore, the final logical effort values for sum and carry for this design are:

- Sum: $g = 1 \cdot 2 \cdot 1 \cdot 2 = 4$
- Carry: $g = 1 \cdot 2 \cdot 1 \cdot 2 = 4$

Design-3 [13], which is shown in Fig. 4, is the same as Design-1, but the only difference is that it uses a 4T XOR logic, which has lesser power dissipation compared to other XOR gates, thus, reducing the total power dissipation compared to Design-1. The circuit on Fig. 4 has four stages

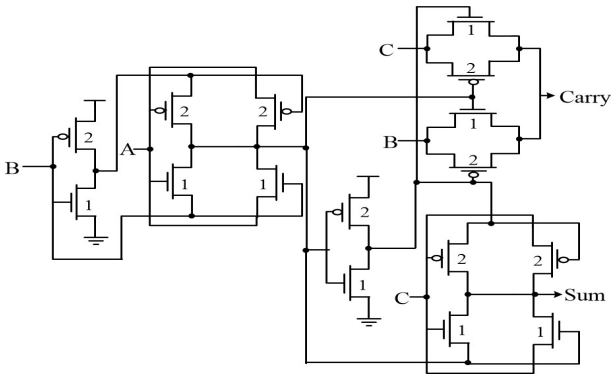

Fig. 3. Low-Power Hybrid Full Adder (Design-2 [14]).

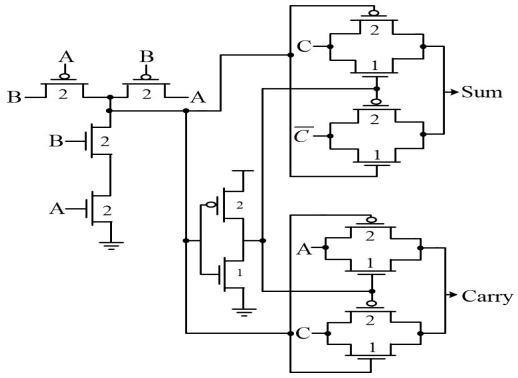

Fig. 4. Low-Power Hybrid Full Adder (Design-3 [13]).

for sum, i.e., XOR with $g = 4/3$, inverter (used for XNOR output) with $g = 1$, inverter (used for input C) with $g = 1$, and multiplexer with $g = 2$. Similarly, it has three stages for carry, i.e., XOR with $g = 4/3$, inverter (used for XNOR output) with $g = 1$, and multiplexer with $g = 2$. Therefore, the final logical effort values for sum and carry are:

- Sum: $g = 1.33 \cdot 1 \cdot 1 \cdot 2 = 2.66$
- Carry: $g = 1.33 \cdot 1 \cdot 2 = 2.66$

As mentioned above, we proposed a new circuit (Fig. 4) in order to get the best delay and much less power dissipation. This design used a 4T XOR gate, and the output of it is connected to an inverter to produce XNOR output. A multiplexer (based on pass transistor logic style) with XOR and XNOR as select lines are used produce carry output, and an XNOR module from Design-3 is used to produce output of sum. This design has three stages for both sum and carry, but sum has XOR which gives $g = \frac{4}{3} = 1.33$, inverter (used to get XNOR output) with $g = 1$, and XOR (for generating sum) which gives $g = \frac{(2+1+2+1)}{3} = 2$. For carry, it has XOR which gives $g = \frac{4}{3} = 1.33$, inverter (used to get XNOR output) with $g = 1$, and multiplexer with $g = 2$. So the final logical effort values for sum and carry for this design are:

- Sum: $g = 1.33 \cdot 1 \cdot 2 = 2.66$
- Carry: $g = 1.33 \cdot 1 \cdot 2 = 2.66$

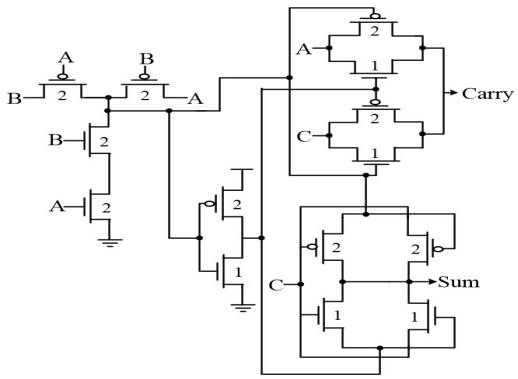

Fig. 5. Proposed Low-Power Hybrid Full Adder (Design-4).

All four designs are simulated using Cadence Virtuoso tool, and their performance is analyzed in terms of power dissipation and delay. The delay of sum and carry for every change

in output (i.e., $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions), average power, power delay product of the sum and carry, and transistor count of all four full adder circuits before resizing (i.e., by taking the default width which is $W = 120nm$ for both NMOS and PMOS), as well as after resizing (i.e., by taking the width $W = 120nm$, where $g = 1$ and $W = 240nm$ with $g = 2$ for both NMOS and PMOS) are listed in Table II. From Table II, it can be observed that the average power, delay, power delay product of sum and carry, and transistor count is minimum for Design-4 before resizing.

Now when, according to logical effort, the full adders are resized, we can see that average power is minimum for the proposed design compared to other three designs, but is higher than the values shown before resizing. This is because, after resizing, the width is increased and so are R and C values. This leads to the power increase.

III. Simulation To Identify Logical Effort And Calculation From Graph

In this investigation, sum and carry for all four architectures are separated and simulated using the 45nm Cadence Virtuoso tool. Initially, the delay is determined from the Cadence Virtuoso tool simulated graph for each circuit and fan-out setting. All the circuits are constructed with the default PMOS and NMOS widths ($W = 120nm$ and $L = 45nm$, respectively). Fan-out from 0 to 4 is taken and the absolute delay for each circuit is determined. Absolute delay is the ratio of any circuit's real delay to the inverter fan-out-0 delay. Table III lists the delay values for logic gates such as inverter, NAND, and NOR (before/after resizing) and for the four designs.

In Table III, the delay values of all circuits are given for fan-out from 0 to 4. From these, we need to calculate absolute delay for all the circuits. The absolute delay values for fan-out 0-4 are listed in Table IV. Now the graph is plotted for each circuit separately. Fan-out from 0 to 4 is plotted in X-axis, and absolute delay values in ps are plotted in Y-axis. The slope is calculated for sum and carry separately in the graph.

Now, if we compare equation (5) with the straight-line equation, which is $y = mx + c$, we can see that absolute delay (d) is plotted in Y-axis, and the electrical effort (h) called fan-out is plotted in X-axis, and the slope (m) gives the logical effort (g) value. The graphs for logic gates and all four designs, including straight-line equations for sum and carry separately, are shown in Figs. 6 and 7. Here, Fig. 6(a) shows the graph of Inverter, NAND and NOR, Fig. 6(b) shows the graph of Design-1, Fig. 6(c) shows the graph of Design-2, Fig. 6(d) shows the graph of Design-3, and Fig. 7 shows the graph of Design-4. As we said, slope value in the straight line equation gives the logical effort value, and the slope is calculated by simulating all the circuits for different fan-out conditions. These slope values are stated as simulated logical effort values. The simulated logical effort values are stated in Table V by comparing them with the calculated logical effort values.

As previously stated, the logical effort value is determined by the slope, and this information is recorded in Table V through comparison with the corresponding calculated values.

In Table V, we can see that the simulated and calculated values have a lot of variations. So, according to the logical effort, the transistors are resized. As the default width for both NMOS and PMOS in 45nm technology is 120nm, the width of PMOS and NMOS are resized according to logical effort values, i.e., width of PMOS is taken as $W = 240nm$ where $g = 2$, and $W = 480nm$ where $g = 4$ the same is done for NMOS. Now, we have to follow the same procedure: the first delay is noted from simulated graph, which is shown in Table V, and absolute delay values are shown in Table IV.

Now the graphs are plotted for all the circuits, which are shown in Figs. 8 and 9. Here, Fig. 8(a) shows the graph of Inverter, NAND and NOR, Fig. 8(b) shows the graph of Design-1, Fig. 8(c) shows the graph of Design-2, Fig. 8(d) shows the graph of Design-3, and Fig. 9 shows the graph of Design-4.

The presented graphs indicate that the slope values have been identified as simulated logical effort values after resizing in Table V in comparison with calculated values of logical effort.

From Table V we can see that the simulated values before resizing have a lot of variations compared to the values after resizing. After resizing the gates, we can see that the calculated and simulated values are almost getting the same.

We have conducted a comparative analysis of the logical effort values and delay times of the fundamental gates after resizing the transistor sizes, as demonstrated in Tables VI and VII in reference to the existing work [16]–[18]. In reference to [17], the author did not provide separate calculations for the PDP and power of the 2-input NAND, NOR, and inverter. Instead, they focused on deriving expressions for the proposed Equal Effect Delay and Voltage Scaling (EEDVS) technique's power, delay, and PDP in comparison to other technologies, specifically UMC 130nm and P45-nm. It is noteworthy that within this technique, the supply voltage has been scaled in accordance with the employed logical effort stages. It is important to note that due to disparities in the underlying technologies utilized in these designs, a direct one-to-one comparison may not be straightforward. Consequently, we have presented the values as reported in the literature. Given that these are fundamental gates, any disparities arising from technological differences are anticipated to be relatively minor, thus preserving the validity of our comparative assessment.

IV. Results Analysis and Discussion

In our work, we utilized the Cadence GPDK 45nm technology node, a widely accepted and extensively verified standard for semiconductor process technology. Its well-established status ensures a high level of confidence in the accuracy and reliability of the provided model libraries. The model libraries associated with the GPDK 45nm technology node have undergone rigorous testing and verification procedures. This extensive validation process covers a wide range of operating conditions and scenarios, bolstering the credibility of our simulations. In our study, we decided to employ the GPDK 45nm technology, primarily due to its wide acceptance and robust design ecosystem, particularly within academic settings.

TABLE II
COMPARISON OF DELAY, AVG. POWER, PDP (POWER DELAY PRODUCT) AND TRANSISTOR COUNT OF ALL FOUR DESIGNS BEFORE/AFTER RESIZING

	Design-1 [5]		**Design-2 [14]**		**Design-3 [13]**		**Design-4 [proposed]**	
	Before	After	Before	After	Before	After	Before	After
Delay of Sum(ns)								
001-(0 $\rightarrow$ 1)	0.039	0.038	0.043	0.044	0.034	0.034	0.033	0.029
011-(1 $\rightarrow$ 0)	0.045	0.056	0.023	0.024	0.050	0.046	0.053	0.047
100-(0 $\rightarrow$ 1)	0.005	0.005	0.006	0.005	0.005	0.004	0.004	0.004
101-(1 $\rightarrow$ 0)	0.029	0.030	0.032	0.044	0.028	0.030	0.040	0.048
111-(0 $\rightarrow$ 1)	0.035	0.043	0.032	0.035	0.040	0.035	0.041	0.037
Delay of Carry(ns)								
011-(0 $\rightarrow$ 1)	0.0344	0.0419	0.0326	0.0340	0.0394	0.0343	0.0461	0.040
100-(1 $\rightarrow$ 0)	0.0049	0.0053	0.0114	0.0159	0.0048	0.0050	0.0048	0.005
101-(0 $\rightarrow$ 1)	0.0061	0.0062	0.0272	0.0308	0.0052	0.0050	0.0054	0.005
Average Power(nW)	75.97	112.5	55.36	82.37	50.42	77.71	47.61	73.32
PDP of Sum ($\times 10^{-18} J$)	0.3798	0.54	0.3266	0.4118	0.2470	0.3496	0.2094	0.3010
PDP of Carry ($\times 10^{-18} J$)	0.3722	0.5962	0.6311	1.3096	0.2420	0.3885	0.2285	0.3812
Transistor Count	20	20	16	16	16	16	14	14

TABLE III
DELAY OF CIRCUITS (PS) FOR FAN-OUT 0-4 BEFORE /AFTER RESIZING

h	**0**		**1**		**2**		**3**		4	
	Before	After	Before	After	Before	After	Before	After	Before	After
Inverter	6.5	6.9	15.8	16.4	19.9	20.6	23.8	24.7	27.7	28.7
NAND	12.6	12.6	30.4	30.9	40.6	41.8	50.5	52.2	60.2	62.5
NOR	5.7	7.2	32.3	25.4	38.7	32.6	45.4	39.5	52.2	46.2
Design-1 SUM [5]	11.1	11.6	63	63.9	94.4	91.3	123.2	117.7	155.4	141.8
Design-1 CARRY [5]	10.9	7.7	62.2	49.9	90.7	73	117.7	94.6	143.6	116.4
Design-2 SUM [14]	11.4	7.8	55.3	53.5	74.4	78.1	91	102	109.5	125.3
Design-2 CARRY [14]	14.8	13.2	65.7	72	87.6	95.9	103.2	127	122.3	151.2
Design-3 SUM [13]	9.2	10.2	42.2	42.8	60	60	77	76.6	92.9	92.7
Design-3 CARRY [13]	9.4	10.3	42.5	42.2	59.4	58.5	75.8	74	91.1	89
Design-4 SUM [Proposed]	7.8	9.2	36.4	38.3	48.7	51.9	63.7	65.2	74.9	78
Design-4 CARRY [Proposed]	9.4	10.3	42.5	422	59.4	58.5	75.8	74	91.1	89

Transistor resizing plays a crucial role in optimizing the delay of the proposed hybrid full adder circuit within the context of the chosen technology.

- By resizing transistors, we effectively alter their width-to-length ratios. This adjustment directly impacts the intrinsic capacitance of the transistors. Specifically, increasing the width relative to the length can result in a reduction of intrinsic capacitance, which, in turn, accelerates the charging and discharging processes during signal propagation.
- Transistor resizing allows for a careful balance between driving strength and capacitive load.
- In advanced technology nodes, interconnect resistance (R) and capacitance (C) effects can significantly contribute to signal delays. Proper transistor resizing helps to mitigate these RC delays by adjusting the driving strength to adequately overcome the capacitive load while minimizing resistance-induced delays.
- It's important to note that while transistor resizing can improve delay, there is typically a trade-off with power consumption. Over-sizing transistors may lead to higher static power dissipation, necessitating a careful optimization to achieve a balance between performance and power efficiency.
- As technology nodes continue to scale down, transistor dimensions shrink, leading to higher channel resistance. Transistor resizing allows for the adjustment of channel dimensions to maintain optimal performance in the face of these scaling trends.

Table II presents the outcomes acquired prior to and subsequent to the alteration in size of the transistors. The Full-Adder Design-4, as proposed, has demonstrated a minimal power dissipation of 47.61nW prior to resizing. Upon resizing, the power dissipation increased to 73.32nW. Notably, Design-4 employs the fewest number of transistors, totaling 14, in comparison to the other three designs.

Table III gives the delay values before and after resizing the transistors for fan-out 0 to 4 of logic gates like inverter, NAND, NOR and sum, carry of four designs. We can observe that as the fan-out is increasing from 0 to 4, the delay values are also getting increased. Even the absolute delay values before and after resizing the transistors are given in Table IV

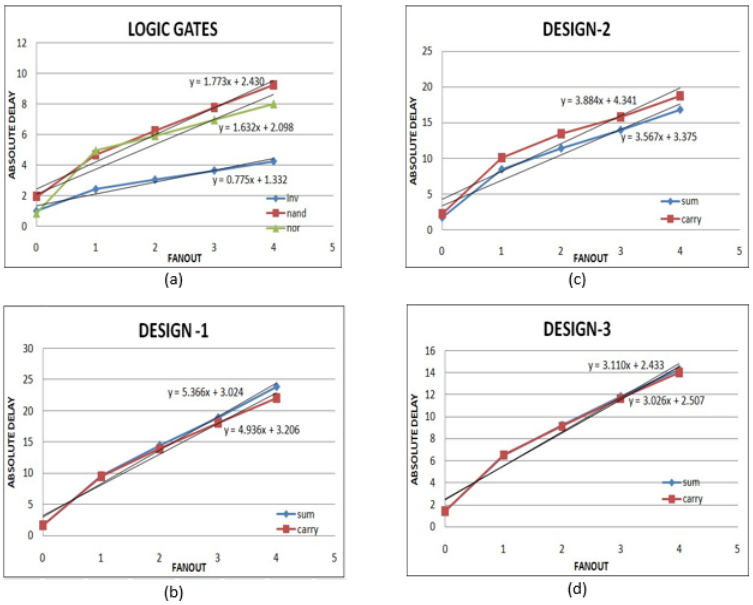

Fig. 6. (a) Fan-out plot vs. Absolute Delay of logic gates; (b) Fan-out plot vs. Absolute Delay of Design-1 [3]; (c) Fan-out plot vs. Absolute Delay of Design-2 [4]; (d) Fan-out plot vs. Absolute Delay of Design-3 [5].

TABLE IV
ABSOLUTE DELAY OF CIRCUITS (PS) FOR FAN-OUT 0-4 BEFORE/AFTER RESIZING

h	0		1		2		3		4	
	Before	After	Before	After	Before	After	Before	After	Before	After
Inverter	1	1	2.43	2.37	3.06	2.98	3.66	3.57	4.26	4.15
NAND	1.93	1.82	4.67	4.47	6.24	6.05	7.76	7.56	9.26	9.05
NOR	0.87	1.04	4.96	3.68	5.95	4.72	6.98	5.72	8.03	6.69
Design-1 SUM [5]	1.70	1.68	9.69	9.26	14.52	13.23	18.95	17.05	23.90	20.55
Design-1 CARRY [5]	1.67	1.11	9.56	7.23	13.95	10.57	18.10	13.71	22.09	16.68
Design-2 SUM [14]	1.75	1.13	8.50	7.75	11.44	11.31	14	14.78	16.84	18.15
Design-2 CARRY [14]	2.27	1.91	10.10	10.43	13.47	13.89	15.87	18.40	18.81	21.91
Design-3 SUM [13]	1.41	1.47	6.49	6.20	9.23	8.69	11.84	11.10	14.29	13.43
Design-3 CARRY [13]	1.44	1.49	6.53	6.11	9.13	8.47	11.66	10.72	14.01	12.89
Design-4 SUM [Proposed]	1.20	1.33	5.60	5.55	7.49	7.52	9.80	9.44	11.52	11.30
Design-4 CARRY [Proposed]	1.44	1.49	6.53	6.11	9.13	8.47	11.66	10.72	14.01	12.89

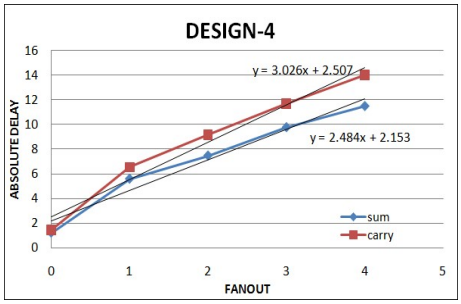

Fig. 7. Fan-out plot vs. Absolute Delay of Design-4 [Proposed].

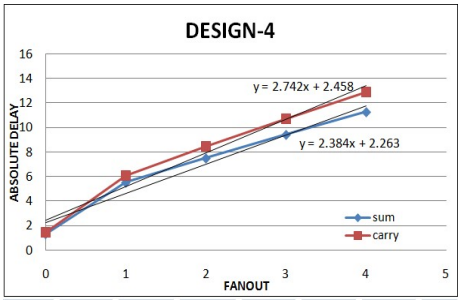

Fig. 8. Fan-out plot vs. Absolute Delay of Design-4 [Proposed].

for fan-out 0 to 4 and the graphs for fan-out vs. absolute delay is plotted for the logic gates, and four full adder designs which are shown in Figs. 6 and 7, and for each graph the line equations are shown. The slope values are noted as simulated logical effort values. Table V gives the comparison of calculated and simulated logical effort values before and after resizing. We can see that there is not much variation between calculated and simulated values of logical effort.

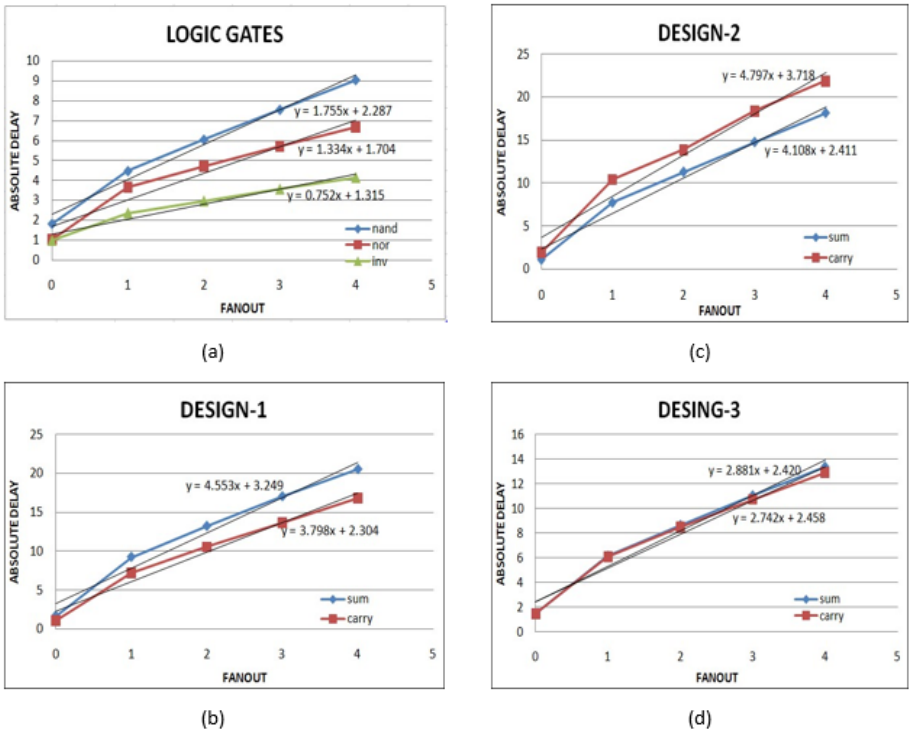

Fig. 9. (a) Fan-out plot vs. Absolute Delay of logic gates; (b) Fan-out plot vs. Absolute Delay of Design-1 [3]; (c) Fan-out plot vs. Absolute Delay of Design-2 [4]; (d) Fan-out plot vs. Absolute Delay of Design-3 [5].

TABLE V
COMPARISON OF CALCULATED AND SIMULATED LOGICAL EFFORT VALUES BEFORE/AFTER RESIZING

Circuit	Calculated Values		Simulated Values (resizing)	
	Before	After	Before	After
Inverter	1	1	0.775	0.752
NAND	1.33	1.33	1.773	1.755
NOR	1.66	1.66	1.632	1.334
Design-1 SUM [5]	4	4	5.366	4.553
Design-1 CARRY [5]	4	4	4.936	3.789
Design-2 SUM [14]	4	4	3.567	4.108
Design-2 CARRY [14]	4	4	3.884	4.797
Design-3 SUM [13]	2.66	2.66	3.110	2.881
Design-3 CARRY [13]	2.66	2.66	3.026	2.742
Design-4 SUM [Proposed]	2.66	2.66	2.484	2.384
Design-4 CARRY [Proposed]	2.66	2.66	3.026	2.742

TABLE VI
COMPARISON OF LOGICAL EFFORT

Logical effort					
	Proposed	[16]	[17]		[18]
Technology	GPDK 45nm	UMC 90nm	UMC 130nm	P45	UMC 90nm
Inverter	0.752	0.9714	0.95	1.57	0.9714
NAND	1.755	1.242	1.2	2.1	1.242
NOR	1.334	1.294	1.6	2.6	1.294

TABLE VII
COMPARISON OF DELAY, AVERAGE POWER, AND PDP

	Delay(pS)					Avg.Power(nW)	PDP
	Proposed	[16]	[17]		[18]	Proposed	Proposed nS x nW
Technology	GPDK 45-nm	UMC 90nm	UMC 130nm	P45	UMC 90nm	GPDK 45-nm	GPDK 45-nm
Inverter	4.15	11.81	21.6	40.2	12.42	15.49	0.064
NAND	9.05	-	30.1	56.4	15.79	12.89	0.116
NOR	6.69	-	35.5	66.0	18.39	23.38	0.156
SUM	26.53nS	-	-	-	-	135.33	3590.30
CARRY	38.06nS	-	-	-	-	130.86	4980.53

The graphs are shown in Figs. 8 and 9. The slope values are noted as simulated logical effort values. We can see that the calculated and simulated values of logical effort after resizing the transistors are almost getting matched.

A. Scaling the supply voltage

To ensure a fair comparison, all the existing and proposed (present work) circuits are designed using Generic Process Design Kit (GPDK) with 45 nm CMOS technology and simulated in Cadence Virtuoso using the same test inputs. The ability of design to operate in a wide variety of supply voltages, from 0.8 V to 1.1 V at typical corners (TT) at 27°C, was investigated.The Fig. 10(c) shows all the results. It has been seen that the proposed design (design 4) is showing better performance in terms of average power, delay of sum and delay of carry than other designs by 34.23%, 26.81% and 4.33%, respectively.

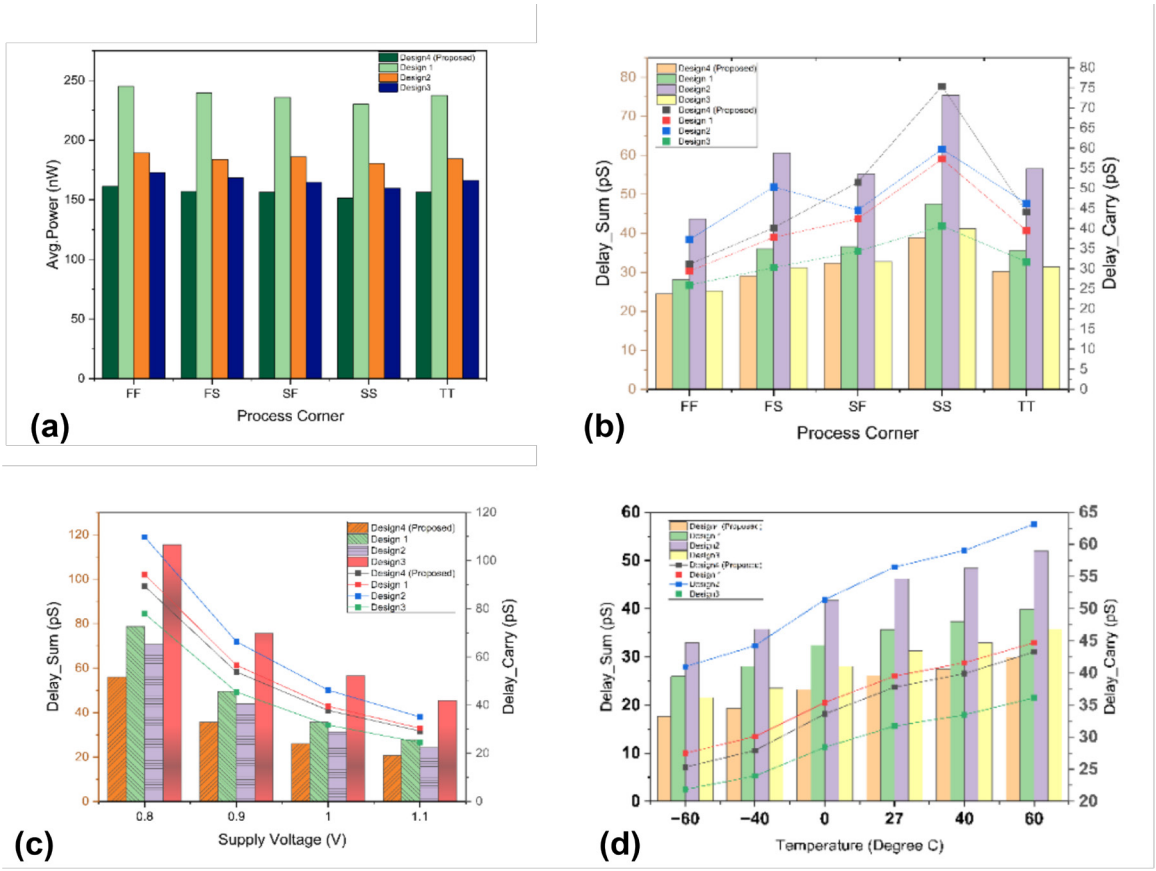

Fig. 10. PVT analysis graphs: (a) average power variation with process corner for all the compared designs, (b) Sum and Carry delay variation with process corner for all the compared designs, (c) sum and carry delay variation with different supply voltage for all the compared designs, and (d) sum and carry delay variation with different temperature for all the compared designs.

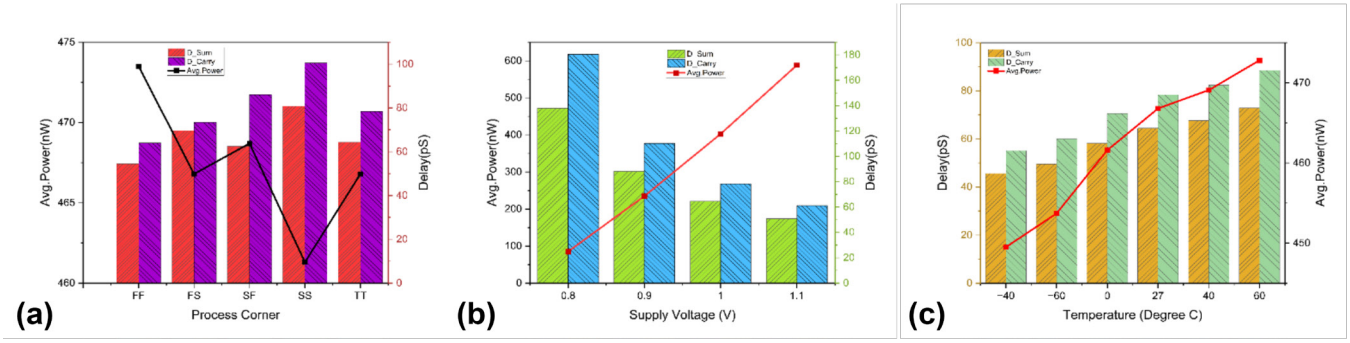

Fig. 11. Post Layout simulation result: (a) average power and Delay of Sum and Carry with variation of process corners, (b) average power and Delay of Sum and Carry with variation of supply voltage, and (c) average power and Delay of Sum and Carry with variation of temperature.

B. Variation in Temperature

The compared designs was also investigated at various temperatures. In Fig. 10(d), the plot of delay for sum and carry over a range of -60°C to +60°C is depicted. Although the power seems to increase with temperature, delay does not increase that much, and hence the PDP is seen to be improved monotonically.

TABLE VIII
COMPARATIVE RESULTS OF POST-LAYOUT MONTE CARLO SIMULATION FOR 1000 ITERATIONS

Design	Delay				SER (%)
	Min (ns)	Max (ns)	Mean (ns)	Std.Dev (ps)	
Design-4 SUM(Proposed)	55.94	83.13	65.20	3.795	0
Design-4 CARRY (Proposed)	67.01	96.77	78.88	4.296	0
Area	l= 3.945 μ m , w= 3.18 μ m,A=12.54 μ m ^{2}				

TABLE IX
COMPARATIVE RESULTS OF MONTE CARLO SIMULATION FOR 1000 ITERATIONS

Design	Delay				SER (%)
	Min (ns)	Max (ns)	Mean (ns)	Std. Dev (ps)	
Design-1 SUM [5]	31.37	43.11	35.97	1.758	0
Design-1 CARRY [5]	33.32	48.99	42.63	1.66	0
Dsign-2 SUM [14]	34.47	50.37	42.14	1.949	0
Dsign-2 CARRY [14]	28.97	38.12	33.02	1.568	0
Dsign-3 SUM [13]	27.94	36.53	31.61	1.412	0
Dsign-3 CARRY [13]	28.37	37.31	32.06	1.467	0
Design-4 SUM (Proposed)	21.86	34.22	26.53	1.76	0
Design-4 CARRY (Proposed)	32.37	45.75	38.06	1.991	0

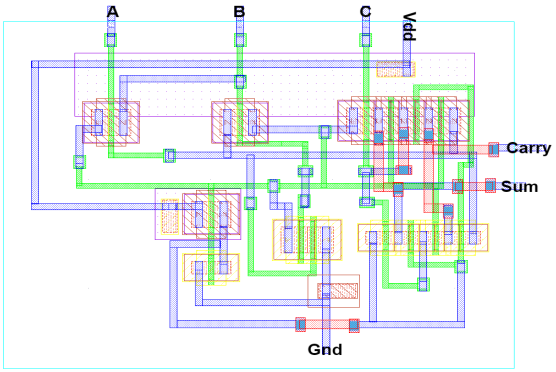

Fig. 12. Layout of proposed full adder circuit [Design-4].

C. Impact of Process Corner Variation

The designs are realized in nanoscale CMOS technology, so it is necessary to check for deviations at process corners considering typical performance metrics. All the designs are analyzed under different process corners and Fig. 10 (a) and (b) shows the result of all the analysis.

D. Verification of Stability using the Monte-Carlo Method

The functional stability of the suggested design is additionally validated through the use of a number of different mismatch and process combinations tested with the Monte Carlo sampling method across 1,000 iterations. The result of the simulation is tabulated in the Table IX.

E. Post-layout Simulation Result

The layout of the proposed design is shown in the Fig. 12 the area and post layout Monte Carlo simulation results are tabulated in the Table VIII. Fig. 11 depicts the post layout PVT simulation results. It can be seen clearly from the result that the proposed design shows better performance than existing full adder designs.

V. CONCLUSION

A low power high-speed hybrid full adder circuit is proposed in this paper and compared this circuit with three existing low power full adder circuits. The simulation was performed in cadence virtuoso tool with gpdk 45nm CMOS technology. The performance of these full adders are analyzed in terms of delay, average power, power delay product, and transistor count. The logical effort method is used to calculate the delay. Simulation is performed with fan-out values from 0 to 4 to find the logical effort required. The transistors are resized to get the best delay according to the logical effort, and comparisons are done.

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