Editor's Column

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> To have friends means to accept that there are more beautiful, smarter, and better people than you. Those, who cannot accept that, have no friends.
>
> *Duško Radović*

Editorial Letter
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THIS year and June issue of the journal we start with three papers focused on design of digital electronics circuits.

In the first paper, entitled "An Approach to Design a Low Power High-Speed Full Adder Circuit Based on Logical Effort," authored by S. Goswami, V. Chandana, and A. Dandapat, authors proposed a low-power full adder circuit and compared it with three established low power full adders. All the circuits were designed utilizing Cadence Virtuoso software and GPDK 45nm technology and comparison was based on delay, average power, power-delay product, and transistor count. Presented results demonstrates that the proposed design brings better performance than other designs in terms of average power, delay of sum, and delay of carry for 34.23%, 26.81%, and 4.33%, respectively.

The paper entitled "A Novel Separable Convolution Architecture for Image Processing Applications," by J. Hassan and B. Khurshid, presents a novel separable Convolution architecture based on the folding transformation that is suitable for image applications, which inherently require efficient two-dimensional (2D) convolution calculation (e.g., image smoothening, image sharpening, feature extraction, image enhancement, object recognition, etc.). The proposed architecture has been implemented in hardware using Xilinx Artix-7 xc7a35tcpg236-1 FPGA device. The results indicate that the implemented solution is beneficial over the existing architectures regarding on-chip resource utilization, power consumption, critical path delay, and external memory bandwidth (EMB).

The last paper, entitled "Accelerated Curve Fitting Approach for Denoised NQR Signal Parameter Estimation," authored by K. Thulasiram Varma and R. Peesapati, demonstrates a feasible approach to extract parameters from exponential decay Nuclear Quadrupole Resonance (NQR) signals using derivative-free optimization approaches on a PYNQ-Z2 FPGA board. As supported by the presented results obtained using the hardware implementation, 0.12 seconds is required to extract the amplitude, frequency, decay constant, and phase from $5 \cdot 10^{-3}$ sec signals with the residual error in the order of 10^{-5}.

Finally, I thank the authors for their contribution to this issue of the journal and send great appreciation to all the reviewers who participated in the editorial process by providing valuable comments in timely manner to the editors and authors.