Testing the Advanced Single Phase Asymmetric Cascaded Multilevel Inverter Topology using RES

Moloy Cgandra Dey, Shamima Akther, Priyangka Talukder, Afshana Begum and Md Moontasir Rashid

***Abstract* — This paper works on developing a model of single phase asymmetrical cascaded multilevel inverter (MLI) which couples' renewable energy sources (RES) to the electrical or electronic loads of the AC powered transport system applications (e.g., Locomotives, Vehicles). MLI is the most important device as it is the main adaptation stage between the source and the load. Researchers are now more focused on multilevel inverters because of its numerous advantages. The prime benefit of a multilevel inverter is obtaining more output voltage levels using a smaller number of DC sources. The proposed topology for this work is asymmetric and produces 31-Levels of output which consists of 12 IGBT switches and 4 isolated dc voltage supplies V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4} (Ratio of 2:4:8:16). The proposed topology has been processed by using PWM (Pulse Width Modulation) technique. Fundamental switching frequency (50HZ) has been used to achieve better quality of output voltage waveform with low harmonic distortion. The proposed topology has been explicitly and thoroughly analyzed throughout the study to demonstrate its superiority over alternative MLI topologies. Power loss analysis of the chosen MLI topology is also shown. An adequate comparison is also carried out between traditional and the proposed topologies. The comparative analysis shows that the chosen existing topology is better performed than others. According to the theoretical analysis conducted, the maximum efficiency obtained is 92.91% along with THD of 4.44% and TSV of 60 V_{dc}. The accuracy of the proposed topology is verified through simulating the entire model in MATLAB-Simulink software.**

***Index Terms*— Multilevel Inverter, MATLAB-Simulink, Renewable Energy, Total Harmonic Distortion**

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I. Introduction

THE multilevel inverter has risen to prominence in the current industry and academic research due to its capacity to provide a high-quality output voltage at a low cost. Multilevel inverters are gaining popularity in a variety of industrial and renewable energy applications these days. In recent years, the number of applications for multilevel power inverters in medium and high-voltage fields has expanded dramatically. The output waveforms of multilevel inverters are better than those of two-level inverters because the output voltage is generated from many levels of dc voltage. This gives rise to a larger focus on multilevel topologies [1]. The fast proliferation of renewable energy systems (RES) is impeding traditional MLI topologies due to performance issues such as low power reliability, an economically unviable structure, and a lack of efficiency [2]. In the cascaded-H Bridge (CHB) topology, a large number of isolated DC power supplies are required, which rises in proportion to the number of levels in the output voltage waveform [3]. Multilevel inverters are designed for applications that require a lot of voltage and power. The key benefits of these inverters include increased output voltage level, lower harmonic content, improved efficiency, and no electromagnetic interference, among others. The waveform of the output voltage is raised. Because the number of steps grows as the number of levels increases, the Total Harmonic Distortion (THD) decreases, making the output waveform more sinusoidal. Raising the level, however, also means increasing the number of switches, making the circuit more complex. For reducing harmonics multilevel inverters require more input voltage sources, so their size is also extended, and it makes the multilevel inverter bulky and costly. To minimize bulkiness and cost, different topologies are nowadays established [4]. Symmetrical and asymmetrical topologies are mainly two types of multilevel inverter topologies. Using asymmetrical topologies, the output voltage levels can be increased so it can easily reduce the THD. If the dc voltage source has varying magnitudes, the inverter output can produce a greater number of voltage levels. The use of an asymmetrical arrangement can reduce the number of power devices and DC voltage sources needed to provide a higher number of various levels of output while also improving efficiency [5]. The focus of this research is to provide a new dc-link topology for an asymmetrical multilevel inverter based on a lower flammable limit that allows for the use of a separate power supply e.g., battery pack, photovoltaic cell, or other renewable sources [6].

II. Proposed Configuration

The internal design of the MLI is the principal focus of this research. Fig. 1 depicts the fundamental idea of how the suggested MLI design can be used efficiently. The renewable energy source (RES e.g., PV Solar Panel) used as a power source to run the MLI which generates direct current (DC) power. The power gained from RES transformed via a DC-to-DC converter and utilized to change the PV voltage and implement the MPPT. The fundamental objective of this research is to create a novel 31-level asymmetrical multilevel inverter topology with the lowest THD and high efficiency. Voltage and current characteristic graphs are a tool for determining and understanding a component's or device's core characteristics, as well as mathematically modeling its behavior inside an electrical circuit such that its voltage and current output graph analysis can be investigated.

The proposed advanced compact DC to AC multilevel inverter with lower THD can be used for the train or vehicle. AC traction is the most often deployed system around the world. Even though solar-powered trains or vehicles rely on sunny weather, in situations when there is insufficient or no direct sunlight, a backup power source, such as a battery, is needed. When there are insufficient solar rays (out of 90-degree angle or bad weather) to power the transit system, the power required for running the system must be supplanted by batteries. There will be several sorts of batteries, which will operate to run the transportation system.

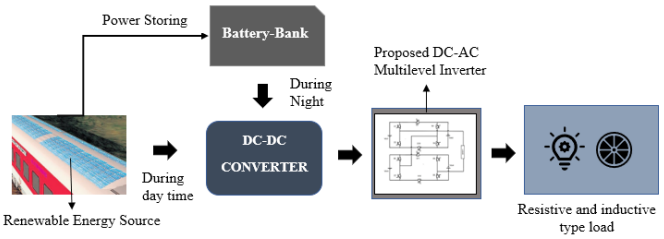


Fig. 1. Proposed block diagram of the coupling arrangement between PV panel and Load

Fig. 2 depicts the proposed asymmetrical circuit topology, which includes 12 unidirectional switches and four independent DC sources. Individual IGBTs are used in the unidirectional switches. *Vdc1, Vdc2, Vdc3,* and *Vdc4* are the magnitudes of four DC sources. The configuration is capable of producing 31-levels in the MLI output. To avoid a short circuit, avoid the conduction of the pairs of switches *S9, S10,* and *S11, S12*. These switches cannot be turned on at the same time.

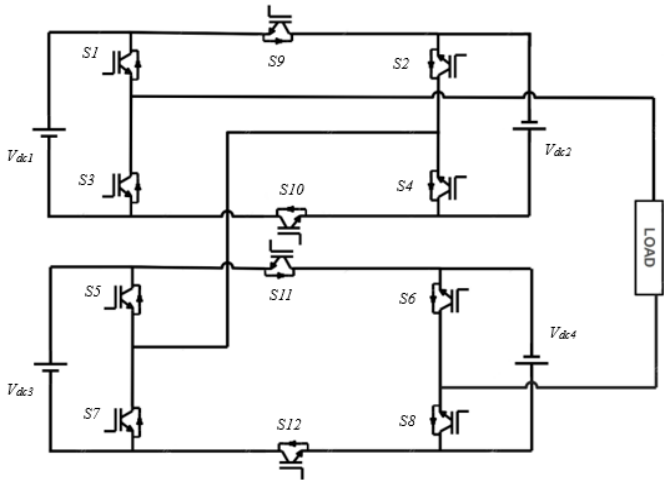


Fig. 2. Proposed circuit diagram of DC-AC Multilevel Inverter

Table. I show various switching states of the proposed MLI, which yields a total of 31-Levels in the output summarized as Positive 15-Levels (0 to +15 V_{dc}), Negative 15-Levels (0 to -15 V_{dc}), and zero level [7].

Table I
Current Direction Path and Active Component

Modes	Current direction of load	Active voltage source	Magnitude of Voltage	Output Voltage
Mode-1	*Vdc1 - S1 - RL - S6 - Vdc4 - S12 - Vdc3 - S5 - S2 - Vdc2 - S10 - Vdc1 - S1 - Vdc1*	*Vdc1 + Vdc2 + Vdc3 + Vdc4*	+15	+30
Mode-2	*Vdc2 - S10 - S3 - RL - S6 - Vdc4 - S12 - Vdc3 - S5 - S2 - Vdc2 - S10 - S3 - Vdc2*	*Vdc2 + Vdc3 + Vdc4*	+14	+28
Mode-3	*Vdc1 - S1 - R0 - S6 - Vdc4 - S6 - S12 - Vdc3 - S5 - S4 - S10 - Vdc1*	*Vdc1 + Vdc3 + Vdc4*	+13	+26
Mode-4	*Vdc3 - S5 - S4 - S10 - S3 - R0 -S6 - Vdc4 - S12 - Vdc3*	*Vdc3 + Vdc4*	+12	+24
Mode-5	*Vdc1 - S1 - R0 - S6 - Vdc4 - S12 - S7 - S2 - Vdc2 - S10 - Vdc1*	*Vdc1 + Vdc2 + Vdc4*	+11	+22
Mode-6	*Vdc2 - S10 - S3 - R0 S6 - Vdc4 - S12 -S7 -S2 - Vdc2*	*Vdc2 + Vdc4*	+10	+20
Mode-7	*Vdc1 - S1 - R0 - S6 - Vdc4 - S12 - S7 - S4 - S10 - Vdc1*	*Vdc1 + Vdc4*	+9	+18
Mode-8	*Vdc4 - S12 - S7 - S4 - S10 - S3 - R0 - S6 - Vdc4*	*Vdc4*	+8	+16
Mode-9	*Vdc1 - S1 - R0 – S8 – S12 - Vdc3 – S5 – S2 – Vdc2 – S10 – Vdc1*	*Vdc1 + Vdc2 + Vdc3*	+7	+14
Mode-10	*Vdc2 – S10 – S3 – R0 – S8 – S12 – Vdc3 – S5 – S2 – Vdc2*	*Vdc2 + Vdc3*	+6	+12
Mode-11	*Vdc1 – S1 – R0 – S8 – S12 – Vdc3 – S5 – S4 – S10 – Vdc1*	*Vdc1 + Vdc3*	+5	+10
Mode-12	*Vdc3 – S5 – S4 – S10 – S3 – R0 – S8 – S12 – Vdc3*	*Vdc3*	+4	+8
Mode-13	*Vdc1 – S1 – R0 – S8 – S12 – S7 – S2 – Vdc2 – S10 – Vdc1*	*Vdc1 + Vdc2*	+3	+6
Mode-14	*Vdc2 – S10 – S3 – R0 – S8 – S12 – S7 – S2 – Vdc2*	*Vdc2*	+2	+4
Mode-15	*Vdc1 – S1 – R0 – S8 – S12 – S7 – S4 – S10 – Vdc1*	*Vdc1*	+1	+2

Modes	Current direction of load	Active voltage source	Magnitude of Voltage	Output Voltage
Mode-16	*R0*	*0*	0	0
Mode-17	*Vdc1 – S3 – R0 – S6 – S11 – S5 – S2 – S9 – Vdc1*	*- Vdc1*	-1	-2
Mode-18	*Vdc2 – S9 – S1 – R0 – S6 – S11 – S5 – S4 – Vdc2*	*-Vdc2*	-2	-4
Mode-19	*Vdc1 – S3 – R0 – S6 – S11 – S5 – S4 – Vdc2 – S9 – Vdc1*	*-Vdc1 - Vdc2*	-3	-6
Mode-20	*Vdc3 – S7 – S2 – S9 – S1 – R0 – S6 – S11 – Vdc3*	*-Vdc3*	-4	-8
Mode-21	*Vdc1 - S3 – R0 – S6 – S11 – S3 – S7 – S2 – S9 – Vdc1*	*- Vdc1 - Vdc3*	-5	-10
Mode-22	*Vdc2 – S9 – S1 – R0 – S6 – S11 – Vdc3 – S7 – S4 – Vdc2*	*- Vdc2 - Vdc3*	-6	-12
Mode-23	*Vdc1 – S3 – R0 – S6 – S11 – Vdc3 – S7 – S4 – Vdc2 – S9 – Vdc1*	*-Vdc1 - Vdc2 - Vdc3*	-7	-14
Mode-24	*Vdc4 – S11 – S5 – S2 – S9 – S1 – R0 – S8 – Vdc4*	*-Vdc4*	-8	-46
Mode-25	*Vdc1 – S3 – R0 – S8 – Vdc4 – S11 – S5 – S2 – S9 – Vdc1*	*- Vdc1 - Vdc4*	-9	-48
Mode-26	*Vdc2 – S9 – S1 – R0 – S8 – Vdc4 – S11 – S5 – S4 – Vdc2*	*- Vdc2 - Vdc4*	-10	-20
Mode-27	*Vdc1 – S3 – R0 – S8 – Vcd4 – S11 – S5 – S4 – Vdc2 – S9 – Vdc1*	*-Vdc1 - Vdc2 - Vdc4*	-11	-22
Mode-28	*Vdc3 – S7 – S2 – S9 – S1 – R0 – S8 – Vdc4 – S11 – Vdc3*	*- Vdc3 - Vdc4*	-12	-24
Mode-29	*Vdc1 - S3 – R0 – S8 – Vdc4 – S11 – Vdc3 – S7 – S2 – S9 – Vdc1*	*-Vdc1 - Vdc3 - Vdc4*	-13	-26
Mode-30	*Vdc2 – S9 – S1 – R0 – S8 – Vdc4 – S11 – Vdc3 – S7 – S4 – Vdc2*	*- Vdc2 - Vdc3 - Vdc4*	-14	-28
Mode-31	*Vdc1 – S3 – R0 – S8 – Vdc4 – S11 – Vdc3 – S7 – S4 – Vdc2 – S9 – Vdc1*	*-Vdc1 - Vdc2 - Vdc3 - Vdc4*	-15	-30

III. Circuit Diagram and Simulation

The proposed topology's performance is validated using MATLAB/Simulink. It can display a graphical depiction of the suggested topology in the Simulink interface. The DC to AC MLI topology is made up of two blocks. For the sake of simplicity, instead of using Solar PV, similar types of constant DC voltage sources are used. These voltage sources represent flow coming from the DC-to-DC converter in the adaptation stage. In this configuration, 12 IGBT switches, 4 DC sources, and 1 load have been used. Each block contains 6 switches and 2 voltage sources of opposite signs. The switches fundamentals are bidirectional and unidirectional. Switches *S1* through *S8* operate for both positive and negative half cycles, while switches *S9* and *S11* operate for positive half cycles and switches *S10* and *S12* for negative half cycles. Fig. 3 depicts the interface of the proposed topology simulation.

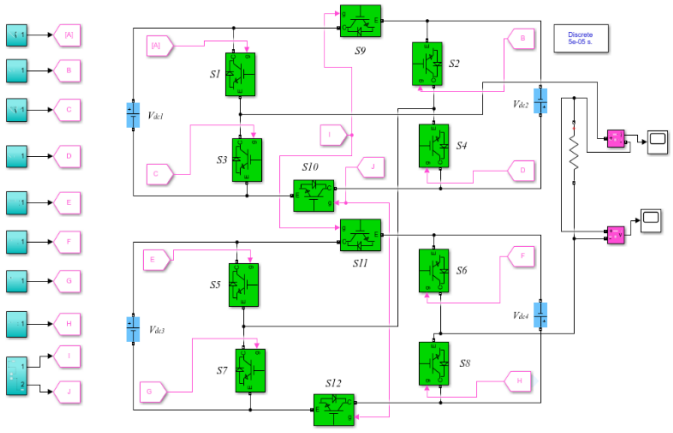
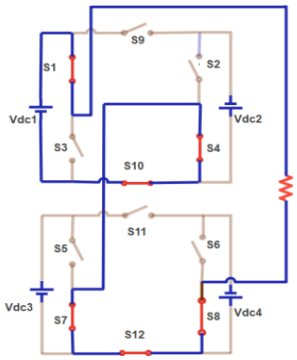


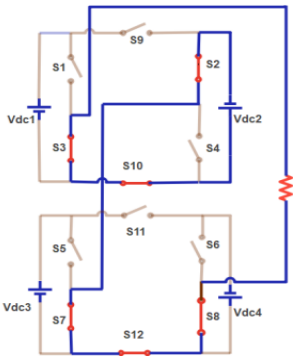
Fig. 3. Simulink Model of 31-Level Asymmetrical MLI

IV. Modes of Operation

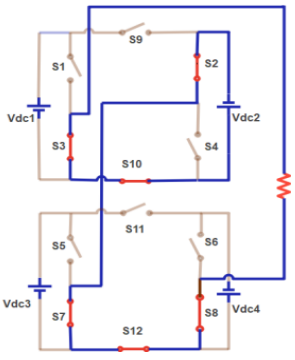
As described in Table. 1, Fig. 4 shows all the connection diagram for positive half cycle voltage. While taking the output, the voltage sources for each mode are maintained on.



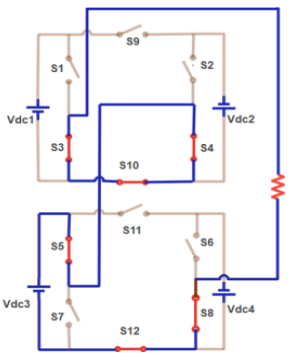
Mode 1: V_{dc1}



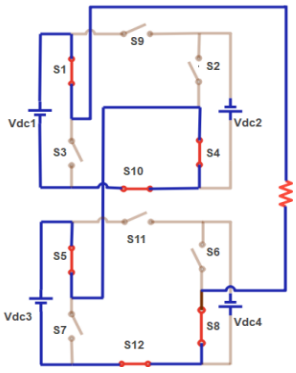
Mode 2: V_{dc2}



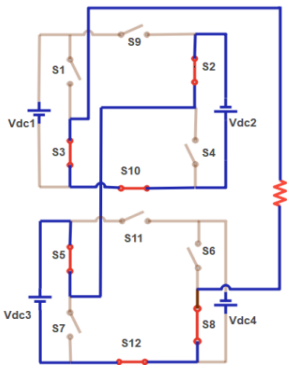
Mode 3: V_{dc1}+ V_{dc2}



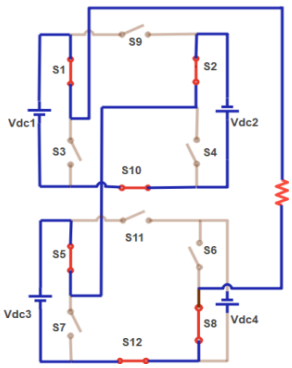
Mode 4: V_{dc3}



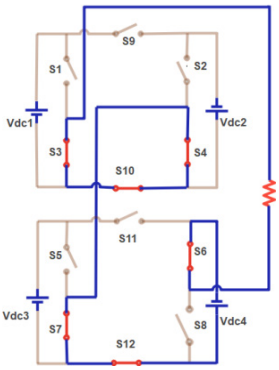
Mode 5: $V_{dc1}+ V_{dc3}$



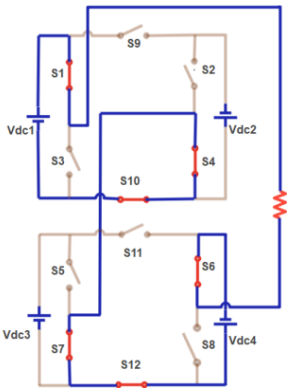
Mode 6: $V_{dc2}+ V_{dc3}$



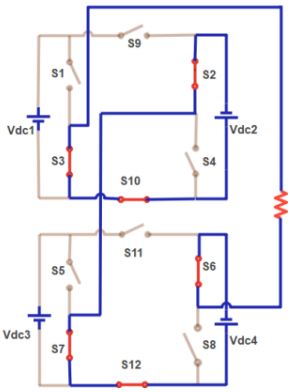
Mode 7: $V_{dc1}+ V_{dc2} + V_{dc3}$



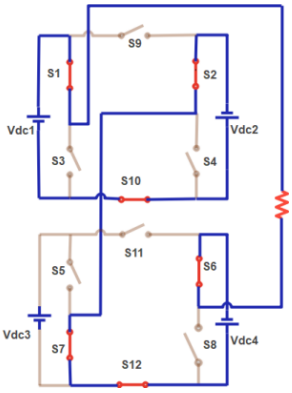
Mode 8: V_{dc4}



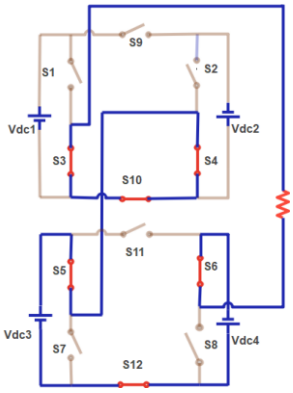
Mode 9: $V_{dc1}+ V_{dc4}$



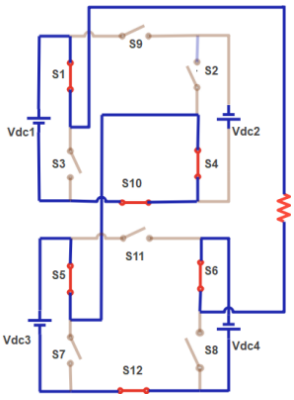
Mode 10: $V_{dc2}+ V_{dc4}$



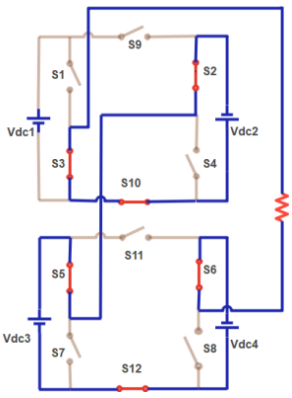
Mode 11: $V_{dc1}+ V_{dc2}+ V_{dc4}$



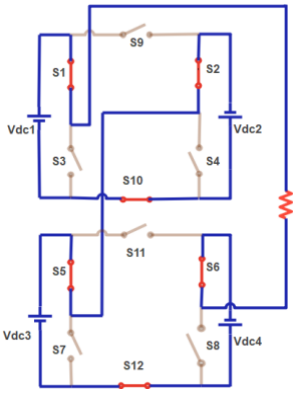
Mode 12: $V_{dc3}+ V_{dc4}$



Mode 13: $V_{dc1}+ V_{dc3} + V_{dc4}$



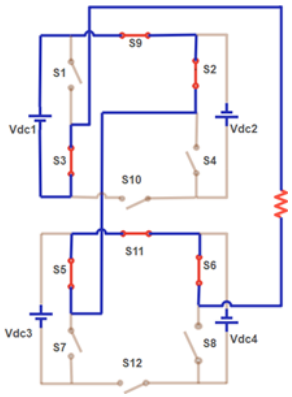
Mode 14: $V_{dc2}+ V_{dc3} + V_{dc4}$



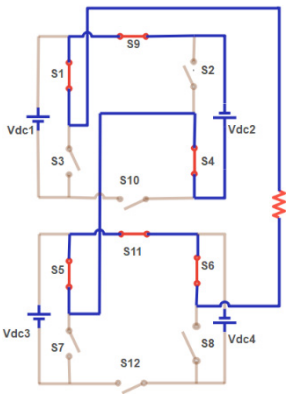
Mode 15: $V_{dc1}+ V_{dc2}+ V_{dc3} + V_{dc4}$

Fig. 4. Connection Diagram of Mode-1 to Mode-15 considering Positive Half Cycle Voltage

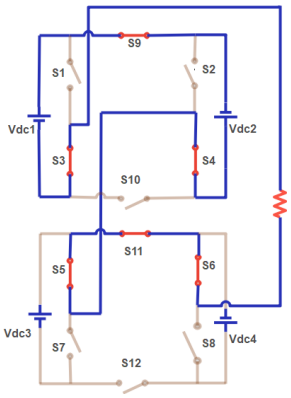
Again, as described in Table. 1, Fig. 5 shows all the connection diagram for negative half cycle voltage, while taking the output, the voltage sources for each mode are maintained on. Mode 16 is 0, hence is not given in the Fig.



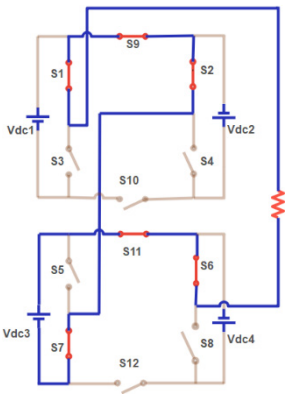
Mode 17: - V_{dc1}



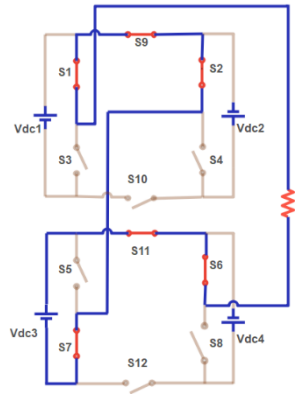
Mode 18: - V_{dc2}



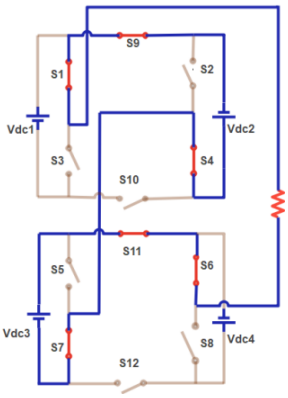
Mode 19: $-(V_{dc1}+V_{dc2})$



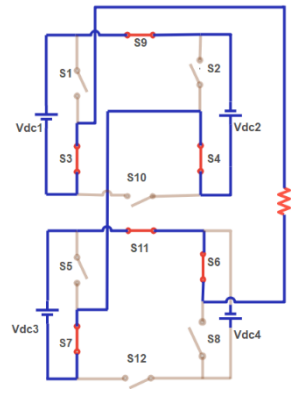
Mode 20: $-V_{dc3}$



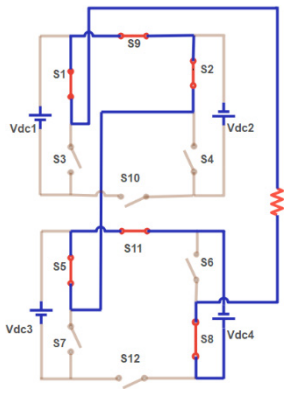
Mode 21:$-(V_{dc1}+V_{dc3})$



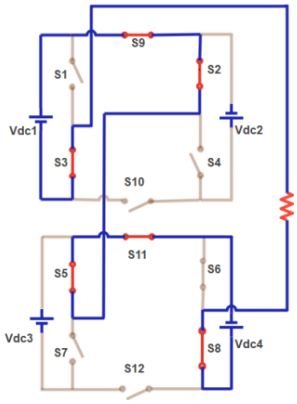
Mode 22: $-(V_{dc2}+V_{dc3})$



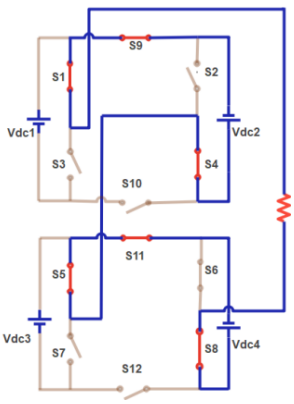
Mode 23: $-(V_{dc1}+V_{dc2}+V_{dc3})$



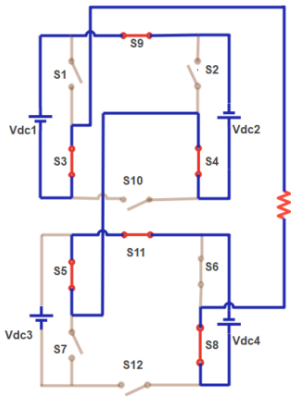
Mode 24: $-V_{dc4}$



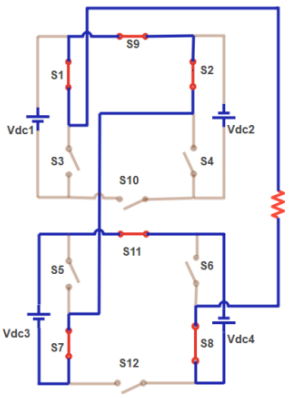
Mode 25: $-(V_{dc1}+V_{dc4})$



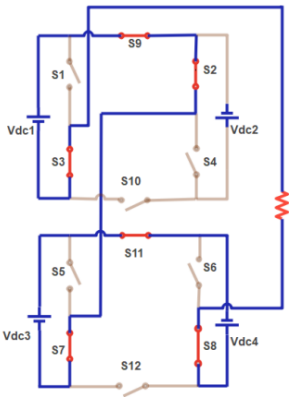
Mode 26: $-(V_{dc2}+V_{dc4})$



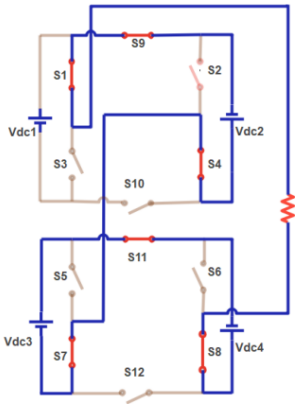
Mode 27: $-(V_{dc1}+V_{dc2}+V_{dc4})$



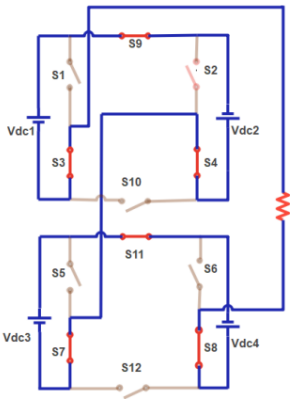
Mode 28: $-(V_{dc3}+V_{dc4})$



Mode 29: $-(Vdc1+Vdc3+Vdc4)$



Mode 30: $-(Vdc2+Vdc3+Vdc4)$



Mode 31: $-(V_{dc1}+V_{dc2}+V_{dc3}+V_{dc4})$

Fig. 5. Connection Diagram of Mode-17 to Mode-31 considering Negative Half Cycle Voltage

V. Total Standing Voltage (TSV)

Total standing voltage is a significant factor in this topology for evaluating the entire system. This is defined as the sum of the maximum voltage the switch has to adopt during its blocking state known as switching stress to generate the output voltage. Because the TSV is tied to the cost of the MLI, it is always predicted to be lower. The higher the TSV, the higher the cost, which means that the switches used for the MLI must be capable of accepting larger blocking voltage [3], [8]-[10].

For the proposed topology, the voltage stress of each switch was calculated as follows:

V_{TSV} = *Total Standing Voltage*

$S1, S2, S3, \ldots, S12$ = *IGBT Switches*

$$V_{TSV}=S1+S2+S3+S4+S5+S6+S7+S8+S9+S10+S11+S12 \quad (1)$$

Where,

$S1=V_{dc}=V_{dc1}=20$ V

$S2=2V_{dc}=V_{dc2}=40$ V

$S3=V_{dc}=V_{dc1}=20$ V

$S4=2V_{dc}=V_{dc2}=40$ V

$S5=4V_{dc}=V_{dc3}=80$ V

$S6=8V_{dc}=V_{dc4}=160$ V

$S7=4V\_dc=V_{dc3}=80$ V

$S8=8V_{dc}=V_{dc4}=160$ V

$S9=3V_{dc}=V_{dc1}+V_{dc2}=60$ V

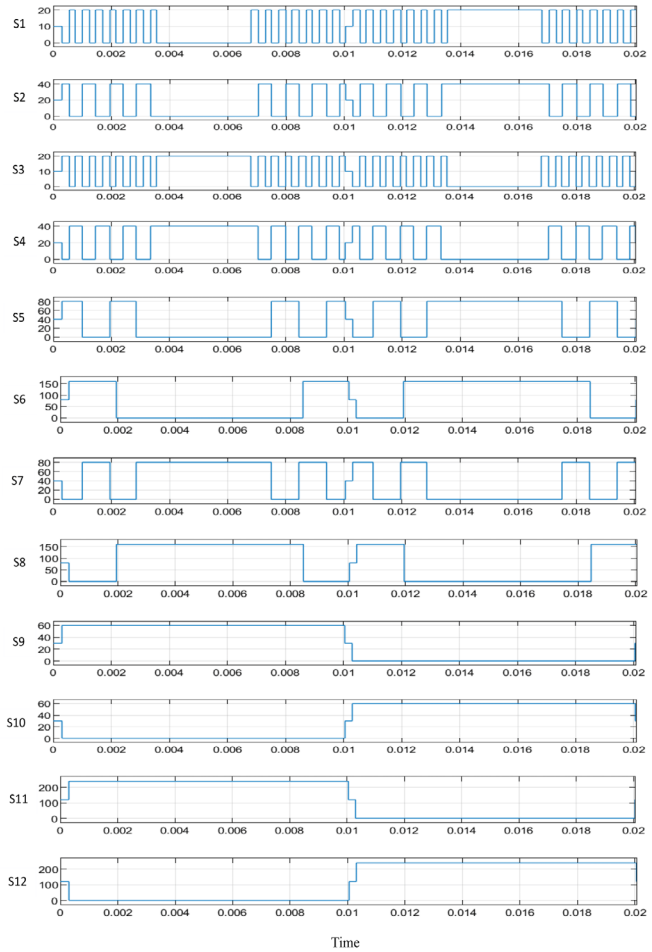


Fig. 6. Switching stress of 12 IGBT switches of 31-Level Proposed MLI

$S10=3V_{dc}=V_{dc1}+V_{dc2}=60$ V

$S11=12V_{dc}=V_{dc3}+V_{dc4}=240$ V

$S12=12V_{dc}=V_{dc3}+V_{dc4}=240$ V

Putting all the values in Equation (1),

$$V_{TSV}=V_{dc}+2V_{dc}+V_{dc}+2V_{dc}+4V_{dc}+8V_{dc}+4V_{dc} +8V_{dc}+3V_{dc}+3V_{dc}+12V_{dc}+12V_{dc}=60V_{dc}$$

The switching stress and staircase modulated output voltage are shown in Fig. 6 and 7. Fig. 6 depicts the stress pulses of 12 switches versus time consumption. Fig. 7 depicts a staircase modulated output versus switching angles [11].

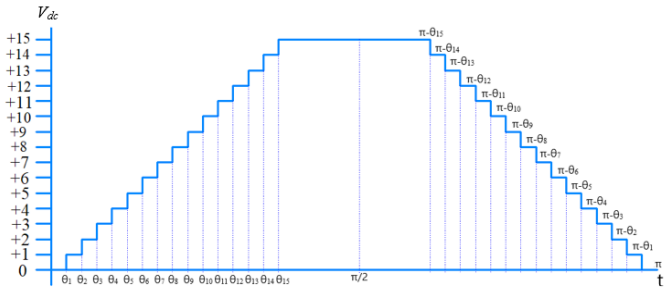


Fig. 7. Staircase modulated output voltage

VI. EXPERIMENTAL RESULTS

A. *Power Loss and Efficiency Analysis*

The power loss of any inverter may be calculated by adding the inverter's conduction loss and the loss of the individual IGBTs employed in that inverter from equation 2. The mathematical expression for calculating inverter conduction loss is the product of voltage () and current () during the conduction period of IGBTs, and the energy loss of each IGBT during on and off states is known as switching loss, which can be determined by the equation 3 [4],[12]. The conduction loss is stated for the summation of on-state and off-state losses of the switches. The efficiency in equation 5 represents a device's operating capabilities, and it can be extrapolated that the higher the efficiency, the higher the productivity [7]. The conduction loss is stated for the summation of on-state and off-state losses of the switches.

$$P_{Cl,IGBT(t)}=[V_{IGBT}+R_{IGBT}+i^{\alpha}(t)]\ \ i(t) \quad (2)$$

$$P_{Cl}=f\sum_{K=1}^{N_{switch}}[\sum_{J=1}^{N_{on,K}}E_{n\ ON,Kj}+\sum_{J=1}^{N_{off,K}}E_{n\ OFF,Kj}] \quad (3)$$

Where, $E_{n\ ON}$ = *Turn – On Losses*

$E_{n\ Off}$ = *Turn– Off Losses*

The total power loss equation as follows:

$$P_{total\ loss} = P_{cl} + P_{sl} \quad (4)$$

P_{cl} = *Conduction Loss*

P_{sl} = *Switching Loss*

Equation of Inverter Efficiency (η) is shows below,

P_{in} = *Input Power*

P_{out} = *Output Power*

$$\eta = \frac{P_{out}}{P_{in}} \quad (5)$$

$$P_{in} = P_{out} + P_{total\ loss} \quad (6)$$

$$\eta = \frac{P_{out}}{P_{out} + P_{total\ loss}} \quad (7)$$

B. *Efficiency Calculation*

The following parameters are extracted from the IGBT APT25GT120BRG data sheet [21]:

$V_{switch} = 0.6$ V

$R_{IGBT} = 0.36\ \Omega$

Turn-On delay time = 14 ns (max)

Turn-On rising time = 27 ns (max)

Turn-Off delay time = 150 ns (max)

Turn-Off fall time = 36 ns (max)

Number of switches = 12

Steps in one full cycle = 86

The output power can be calculated as follows:

$$P_{rms} = V_{\text{rms}} \cdot I_{\text{rms}} \quad (8)$$

Here,

V_o and I_o represent the peak voltage and current respectively. Those values are found in the MATLAB SIMULATION graph 9 (c) and 9 (d) respectively [4].

$V_o = 310$ V

$R_o = 100\ \Omega$

$I_o = 3.1$ A

$$V_{rms} = 0.707 \cdot V_o = 0.707 \cdot 310\ \text{V} = 219.17\ \text{V} \quad (9)$$

$$I_{rms} = 0.707 \cdot I_{rms} = 0.707 \cdot 3.1\ \text{A} = 2.1917\ \text{A} \quad (10)$$

The conduction losses are calculated as follows:

$$P_{cl} = [V_{switch} + R_{IGBT} \cdot I_{rms}] \cdot I_{rms} \cdot no.of\ switches = (0.6 + 0.36 \cdot 2.1917) \cdot 2.1917 \cdot 12\ \text{W} = 36.5316\ \text{W} \quad (11)$$

$$E_{nON} = 219.17 \cdot 2.1917[(14 + 27) \cdot 10^{-9}] \cdot 86 \cdot 12 = 0.02032\ \text{W} \quad (12)$$

$$E_{nOFF} = 219.17 \cdot 2.1917[(150+36) \cdot 10^{-9}] \cdot 86 \cdot 12 = 0.0922\ \text{W} \quad (13)$$

The switching losses are calculated,

$$P_{sl} = E_{nON} + E_{nOFF} = 0.02032 + 0.0922\ \text{W} = 0.11252\ \text{W} \quad (14)$$

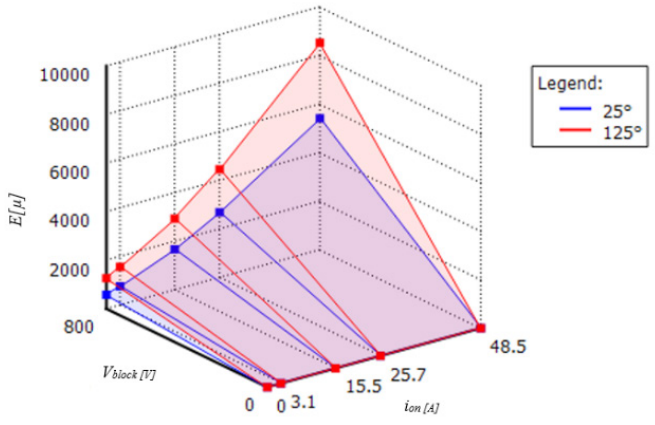
Using equation 4, the total losses during conduction and switching time are determined,

$$P_{total\ loss} = P_{cl} + P_{sl} = 36.5316 + 0.11252\ \text{W} = 36.64412\ \text{W}$$

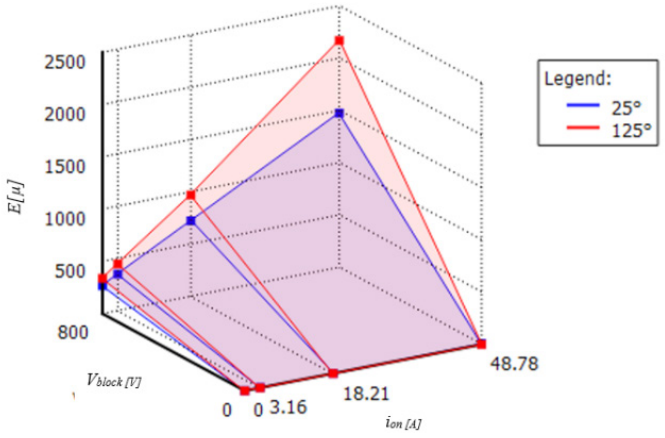
The efficiency is calculated by equation (5),

$$\eta(\%) = P_{\text{out}} / (P_{out} + P_{total\ loss}) \cdot 100 = 480.355/(480.355 + 36.64412) \cdot 100\% = 92.91\%$$

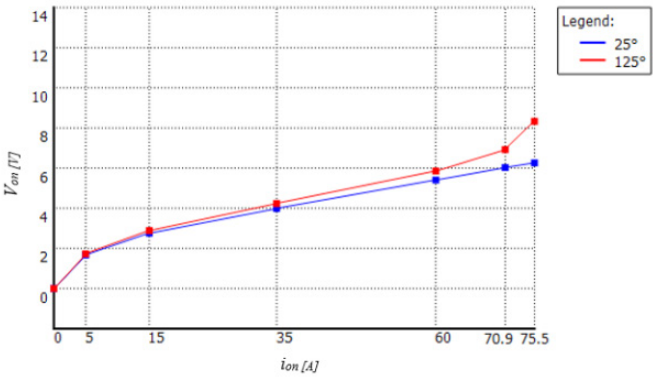
The thermal modeling of conduction loss and switching losses of IGBT on and off states while conducting current is shown in Fig. 6. The thermal models are shown using PLECS (Piecewise Linear Electrical Circuit Simulation) and data from the IGBT APT25GT120BRG data sheet. The correct computation of total energy loss of semiconductors (IGBTs) is based on the thermal graph table and data sheet information. Fig. 8(a), 8(b), and 8(c) models of turn-on loss, turn-off loss, and conduction loss are generated from IGBTs of APT25GT120BRG up to 48.5A, 48.78A, and 75.5A, respectively. The power loss of the developed 31-level asymmetrical inverter under resistive load was investigated.



(a)



(b)



(c)

Fig. 8. Thermal model for (a) turn ON losses, (b) turn OFF losses, and (c) conduction losses for IGBT APT25GT120BRG up to 48.78A, [E = Energy loss (mJ), V_{block} = OFF state blocking voltage (V), I_{ON} = ON state current (A), and V_{ON} = ON state voltage drop (V)]

X. *THD Calculation*

Now the harmonic factor (HF) is expressed as,

$$H_F = H_h / H_1 \tag{15}$$

H_h = All Harmonics

H_1 = First Harmonic

The total harmonic distortion (THD) is,

$$THD(\%) = \sqrt{\sum_{h=2} H_h 2 / H_1} \tag{16}$$

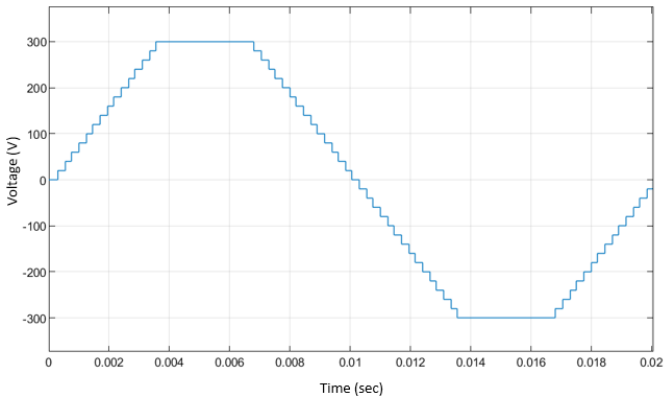
$$= \sqrt{(H_3^2 + H_3^2 + H_3^2 + H_3^2 + H_3^2 + H_3^2 + H_3^2 + H_3^2 + H_3^2 / H_1}$$

$$= \sqrt{1.77^2 + 3.19^2 + 2.28^2 + 0.62^2 + 0.48^2 + 0.65^2 + 0.4^2 + 0.15^2 / 100}$$

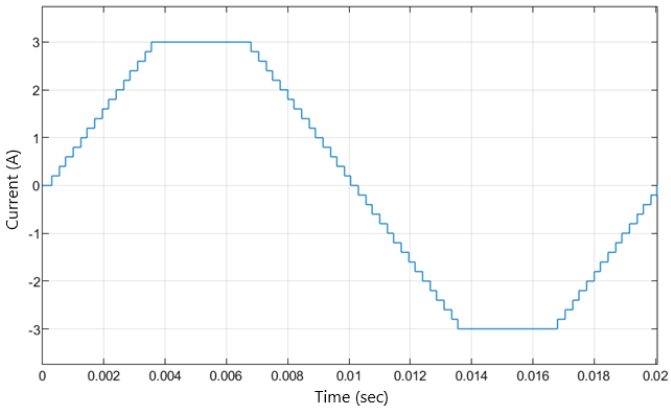
$$= 4.44\%$$

VII. Simulation Result and Discussion

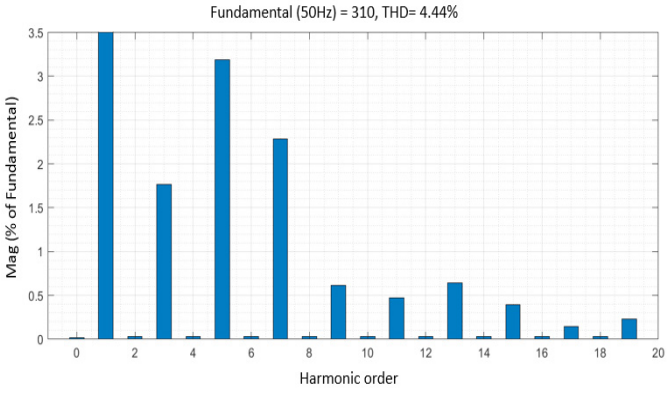
To validate the accuracy of the proposed 31-level asymmetrical multilevel inverter topology, the MATLAB Simulink (R2020) software was used as the primary simulation software. In the simulation part, IGBT APT25GT120BRG switches are assumed to be used as conduction components [3]. The switches were connected to a 100Ω resistive load. The simulation of this MLI uses a low frequency of 50 Hz. The maximum peak-to-peak output voltage found in the simulation is 600V (300V to -300V) while the smallest peak-to-peak output voltage is 40V (20V to -20V). As a result, the modulation factor is 0.707.



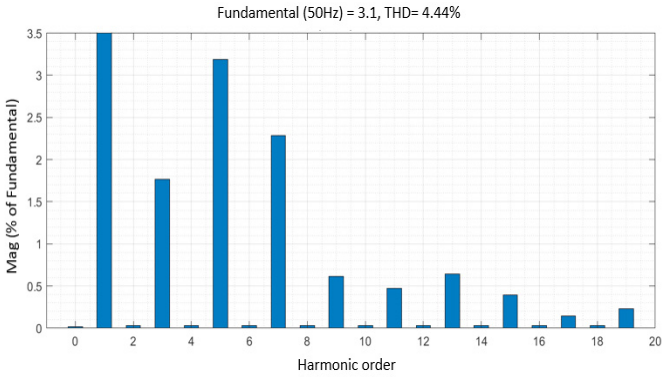
(a)



(b)



(c)



(d)

Fig. 9. (a) The output voltage wave, (b) The output current wave, (c) FFT spectrum of the output voltage and (d) FFT spectrum of output current respectively.

Fig. 9(a) shows that the MATLAB simulation produced a total output of 31. The output took 0.02 seconds to complete one full cycle, as represented in the x-axis of the output voltage wave figure, while the y-axis highlighted the numerical data of output voltage. Fig. 9(b) depicts an output current curve with each step size equal to 0.2A and a peak-to-peak current of 3A to -3A. For one whole cycle, the time remains constant at 0.2 seconds.

Harmonic data spectrums for the developed MLI's output voltage and current are shown in Fig. 9(c) and 9(d) [13]. THD grew by 4.44% (compared to the IEEE standard of 5%) during the simulation period. The individual fifth harmonic is slightly higher than 3%, while the rest harmonics stay below 3% to comply with IEEE standards. The harmonic orders are also visible in the spectrum.

VIII. Comparative Study

To validate the improvement of proposed 31-level inverter topology, comparison has been made with other conventional and other existing asymmetrical multilevel inverter topology in Table. II and Table. III respectively.

Table II
Comparison with Different Types of Conventional MLI

Comparison parameter	CMLI	DCMLI	FCMLI	Proposed
Number of switches	60	60	60	12
Number of dc source	15	1	1	4
Number of levels	31	31	31	31
Clamping diodes	-	56	-	-
Clamping capacitors	-	-	28	-
Driver circuit	60	60	60	10

Dhanamjayulu, C. et al. [4] provided the comparative parameter for several forms of conventional MLI. Table. II shows that the suggested 31-level architecture used the fewest number of components and obtained 4.44% overall harmonic distortion when compared to other typical MLI. The comparison also has been shown in the form of a bar chart in Fig. 10. The chart shows that the proposed model outperforms the other models in terms of employing fewer switches and driver circuits. However, the THD is somewhat higher than CMLI, and the other two were not discussed in the Dhanamjayulu et al. [4] publication.

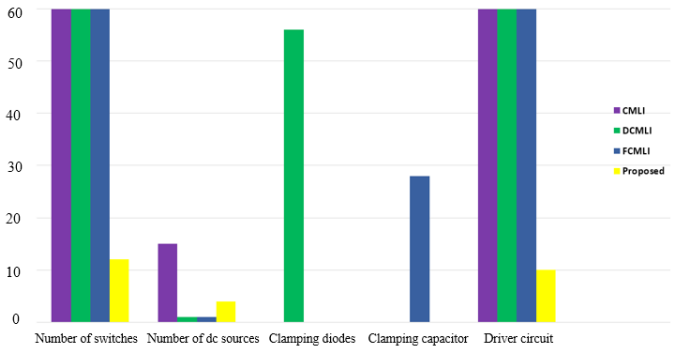


Fig. 10. Bar chart demonstrating comparative analysis of table II

In terms of Table. III, the comparison was made with various 31-level asymmetrical topologies, and the proposed topology obtained overall convincing results. Fig. 11 depicts the comparison of Table. II (a) the number of DC voltage sources and (b) the number of switches versus the number of levels, respectively [6],[14]. Dhanamjayulu C. et al [15] and Mahato, B. et al [17] addressed in their article that they obtained 3.26% and 2.63% respectively, which is lower than what is recorded by the proposed model, but it is clearly stated that the number of switches and dc sources is less, which also consumes less power loss and has a smaller size.

Table III
Comparison Between Proposed and Similar Type Asymmetrical MLI Topologies

Comparison parameter	Gautam,S.P. et el. [16]	Dhanamjayulu, C. et el. [15]	Mahato, B., et el. [17]	Boora, K., et el.[18]	Proposed topology
Number of switches	16	10	10	12	12
Number of dc source	4	6	6	7	4
Number of levels	31	17	31	31	31
Clamping diode	16	-	16	12	-
Driver circuit	16	10	10	12	10
THD	-	4.54%	2.63%	-	4.44%

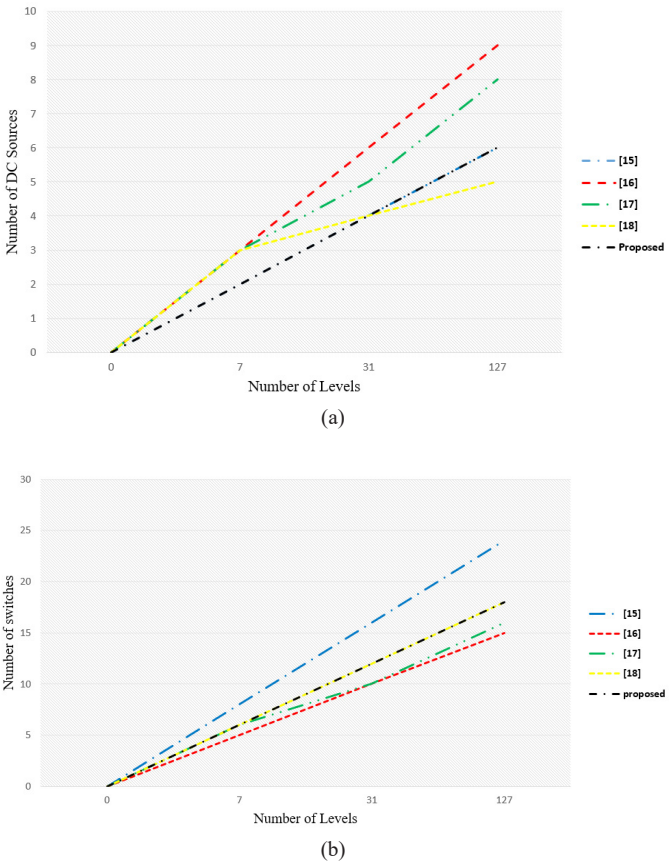


Fig. 11. Line chart demonstration of the comparison for (a) number of DC voltage sources and (b) number of switches versus number of levels

IX. Conclusion

In this study, a new asymmetrical MLI configuration is designed via MATLAB Simulink. The future will be dominated by renewable energy because it is the next generation of energy [19]. Because of the alarming consequences of climate change, the world is currently transitioning to a decarbonized society, which includes every feasible option to decarbonize practically everything. Solar PV is a viable power source among the renewable energy sources. Solar PV, battery mechanisms, MPPT, and converters are all significant considerations. The main topic of this research article was the DC to AC inverter, which is fast, compact, and has low output distortion. The inverter model is designed in such a way that it requires very few switches. After extensive investigation, this tiny inverter can deliver 92.91% efficiency, which is fairly good when compared to other versions. The proposed topology is compared to other conventional and asymmetrical 31-level MLI topologies, which aids in understanding the model's advantages and disadvantages. Higher extension of levels can also be done by following a similar concept [20]. Overall, the proposed topology is a better model that could lower stress over the full adaptation stages coupling the renewable sources to loads.

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