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Editor's Column

Mladen Knezic

> The present is theirs; the future, for which I really worked, is mine.
>
> *Nikola Tesla*

Editorial Letter
DOI: 10.53314/ELS2125001K

ALMOST two years of challenge are behind us. Hopefully, this year we will start returning back to normal life. The time will tell if we learned something or just wasted time as on many occasions before.

In the journal "Electronics", we open this year with four original research papers that provide results in the field of sensor networks, antennas, digital system design, and power electronics.

In the first paper entitled "Energy Optimization in a Multihop Sensor Network for a WBAN Application," authors, V. Tyagi, S. H. Gupta, and M. Kaushik, proposed an energy efficient data transmission for multi-hop network based on Particle Swarm Optimization (PSO) algorithm. The provided results show a significant reduction in energy consumption while keeping the node-to-sink distance constant.

The paper "Dual Notched-Band Crescent Moon Dielectric Resonator Antenna," by M. Debab, A. Bendaoudi, and Z. Mahdjoub, proposes a dual-band notched ultra-wideband (UWB) dielectric resonator antenna. Obtained simulation results demonstrate that the proposed CMDR antenna achieves satisfactory UWB performance, with an impedance bandwidth of around 88.7%, covering the frequency band of 3.2-8.3 GHz, excluding a rejection band for the WLAN and ITU 7 GHz band.

In the paper "On The Implementation of Densely Packed Decimal Number System based Adder: Prospects and Challenges," authored by S. K. Beura, R. U. Ahmed, B. P. Devi, and P. Saha, reports the pros and cons of the Densely Packed Decimal (DPD) coding techniques. Additionally, performance parameters (such as delay, power consumption) have been evaluated through CMOS gpdk45 nm technology.

Finally, the paper "Harmonic Elimination in Uniform Step Nine-Level Inverter Using Differential Evolution: Experimental Validation," by R. F. Abdelgoui, R. Taleb, A. Bentaallah, and F. Chabni, presents the application of differential evolution algorithm for computing optimal switching angles for a single-phase nine-level inverter to improve the output voltage quality. Moreover, the authors built a laboratory prototype based on STM32F407 microcontroller in order to the effectiveness of the proposed modulation method.

I thank the authors for their contribution to this issue of the journal and to all the reviewers who participated in the editorial process by providing valuable comments in timely manner to the editors and the authors.

Energy Optimization in a Multihop Sensor Network for a WBAN Application

Vishakha Tyagi, Sindhu Hak Gupta, and Monica Kaushik

***Abstract*—Movement and posture change of human body plays a crucial role in energy consumption while data transmission between strategically deployed nodes in wireless body area networks (WBANs). The majority of energy is used in transmission rather than processing of the data. Nodes within body are there for long time and need to be energy efficient so that the network lifetime is increased. In this paper, we propose an energy efficient data transmission for multi-hop network that uses particle swarm optimization (PSO) for optimizing the parameters on which energy consumption relies. An energy efficient data transmission and reception takes place by altering the parameters like node to node distance and packet size of data. The obtained results show a significant reduction of energy consumed by reducing the packet size and keeping the node-to-sink distance a constant value. The total energy consumed per hop per bit length of data packet E_{mh}/L shows 75% optimization. The energy consumed in data transmission per bit length of data E_{tx}/L and the energy consumed for data received per bit length of data packet E_{rx}/L is optimized by approximately 70% and 50% respectively for hope count 2 to 5.**

***Index Terms*—Energy Optimization, Forwarder node, Mobility, Multi-hop Communication, Particle Swarm Optimization (PSO), Sensor Network, Wireless Body Area Network (WBAN).**

Original Research Paper
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I. Introduction

Internet of things (IOT) is a system of a variety of things or objects connected through a wireless and self-configurable network [1].

IOT has evolved over the last decade due to convergence of various cutting-edge technologies, real time analytics, machine learning, commodity sensors and traditional fields of embedded systems, Wireless Sensor Network (WSN), control systems, automation and mobile communication [2]. The mobile communication technology and internet plays an important role for setting up a communication channel of smart devices in IOT. WSN refers to a self-configurable and infrastructure-less group of distributed and dedicated sensors for monitoring certain parameters like temperature, sound, humidity etc. and other physical environment conditions, and storing the aggregated data at a central, probably distant location [3].

WBAN, an application of WSN represent promising approaches for improving the patient's quality of life and for health care sector as it consists of multiple sensor nodes deployed in body [4], on body or off the body and each sensor node is capable of sensing, sampling, processing, and communicating vital signs (heart rate, blood pressure, oxygen level, activity, glucose level) [5]. WBAN supports several interesting applications which include areas such as sports, health care, assisted elder care, and response to emergency and diagnostic. Ascending healthcare costs and aging of people around the world has contributed to development in telemedicine network for the delivery of smart health care services [6]. In this type of network, sensors, distributed on the human body, measure several physiological parameters and then transmit the health information, via internet, to a central healthcare system (to an attending physician) or family member in charge. The aggregated data further helps scientific researchers, physicians and other medical personnel to serve more patients [5].

In WBAN, nodes change position due to human body mobility, causing the network topology to rearrange and links between nodes to break and re-establish according to new topology [7]. The continuous monitoring of health information by sensing nodes on human body leads to cutback of the energy of nodes which is a major obstacle in communication between nodes and sink [8] as well as to the longevity of the network. Therefore, sensors parameters, like energy consumption, need to be vital in process of designing sensors.

A general communication WBAN based e-healthcare system architecture is presented in Fig. 1.

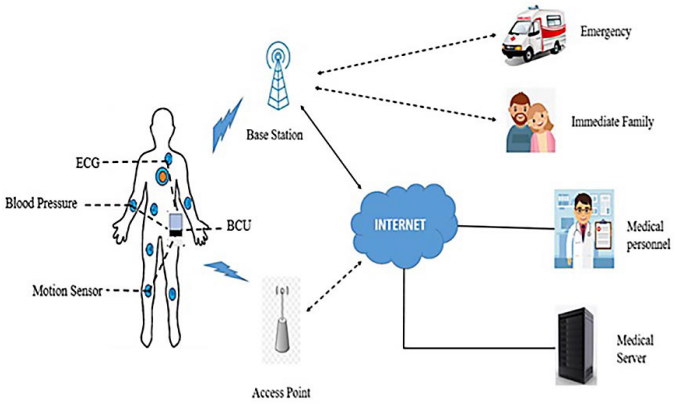

Fig. 1. A generalized architecture of a WBAN-based healthcare monitoring system.

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It comprises of a network of several sensing nodes, a body control unit (BCU) (PDA or a smart phone) linking to another network types (that could be another node with similar features), and a wide network like Internet (via base station) for connecting to medical personnel, family or other healthcare personnel (notifying ambulance in case of emergency).

Sensor nodes collect data on parameters such as electrocardiogram (ECG), photoplethysmogram (PPG), electroencephalography (EEG) pulse, temperature of the body, blood flow, and pressure and glucose level and send it to BCU [9].

Biological and physiological information gathered by the BCU is then transmitted to remote/local destination server marked by a specific patient ID. This data can be processed to obtain accurate estimations of physiological parameters which allow doctors to have real time judgment for medical diagnosis and therapeutic monitoring.

Medical personnel, after analyzing and processing the data, can connect to sensors via sink node and give timely medical services to a patient. A more complex WBAN architecture may have parent node as an intermediating node between senders and sink [10], they are needed when a sensor cannot reach the sink node directly due to the human body mobility and constitution.

Rest of the paper has been structured as follows: Section II presents related work. Energy model is given in Section III. Section IV describes various energy optimization algorithms and the optimization conducted. Results and observations are presented in section V. Section VI features the conclusion of the proposed work.

II. Related Work

In the past few years various models have been proposed and other work has been done related to WSN, WSAN and WBAN. Various approaches have been proposed to make WSN, WBAN energy efficient network, but optimization techniques to optimize energy consumption while keeping in mind the factors on which it depends, have not been explored exhaustively.

In WBAN a significant part of the energy of sensing nodes, is spent in sending and receiving data rather than processing the data. The research work related to the development of routing protocols and use of various optimization techniques in order to make the system more energy efficient when data transmission is in question, has been summarized in Table I. Energy consumption in sensors not only depends on which communication mechanism is followed (single or multi-hop), but also on the distance between nodes, the length of data packet to be sent, transmitting and receiving circuit and path loss factors.

The problem of making nodes energy efficient by keeping node-to-node distance an optimum one and sending data with an optimum length of the packet can be modeled as an optimization problem.

In this proposed work, an energy model has been formulated by considering various parameters like distance between nodes, packet size of data transmitted and energy used for transmission and receiving of data.

TABLE I
Research Work Related to Modelling and Optimization in WBAN

REFERENCE	TARGET	WORK DONE
[4]	A model design of energy-efficient and cost-effective wireless body area networks	Author addresses the topology design problem for WBAN, bearing in mind both the cost and energy issues and offered a novel model centered on mathematical programming that determines the optimum number, assignment of nodes and optimum traffic routing.
[7]	Energy efficient routing protocol.	Authors have proposed an energy effective routing protocol M-TSIMPLE for WBAN taking freedom of movement of nodes into consideration.
[11]	Dynamic Hub selection	Authors have proposed dynamic hub selection in WBAN based on IEEE 802.15.6 in order to mitigate the higher SAR (Specific Absorption Rate) impact resulting due to fixation of HUB in traditional WBAN.
[12]	PSO for relay node placement	Use of PSO for relay node placement on the body is proposed by the authors. Distance between nodes directly affects the energy consumed by the sensors and EMF radiated, thus placement of relay nodes at appropriate distance helps in lowering SAR value and lengthening node lifetime.
[13]	Integrating SDN into WSAN systems.	According to authors, the performance and management services of existing WSAN systems can be enhanced by integrating SDN approach into them. The paper reveals that SDN enabled WSAN performs better than regular zigBee protocol in terms of energy consumption and network flexibility.
[14]	Development of energy efficient routing protocol ESR-W	Authors developed a new energy efficient routing protocol ESR-W using fuzzy based Djikstra technique for SD-WBAN architecture. The new protocol results in improved throughput, end-to-end delay and lesser energy consumption.
[15]	To build an energy aware flexible WSAN architecture	Energy efficiency is a main concern for WSAN, hence the importance of devising efficient architectures. Authors in this paper proposes a new routing decision approach which takes distance between the nodes and remaining energy of the nodes in the path into consideration to prolong the lifetime of network.
[16]	A mathematical model considering human mobility.	A mobility model for the node movements established on different postures made during activities, with multihop and forwarder-based routing schemes has been proposed by and stated that performance of forwarder-based routing schemes is better than the multihop routing scheme.

REFERENCE	TARGET	WORK DONE
[17]	Prolonging the lifetime of WBAN	Authors here investigate energy efficient optimization in WBAN with multi-antenna AP to maximize the rate energy ratio of the system subject to SINR.
[18]	Efficient Energy Consumption Model	A system level energy consumption model for on-body wireless communication has been proposed related to distance and data rate of transmission and transmission, considering energy consumption by circuit and in transmission.
[19]	A routing protocol for stable energy use.	A unique routing protocol for stable energy consumption using multi-hop routing technique for static condition has been suggested.
[20]	Energy optimization	Global energy optimization (GEM) model is optimized for energy based on the quality of service (QoS).

III. Energy Model

WBAN consists of a number of nodes which are battery driven but with limited energy. The energy constraint, in turn, limits the transmission energy for sending the data from node to node. Therefore, the data sent by a node reaches the sink node through multiple hops. In a WBAN, the communication can either be a single-hop communication or multi-hop communication.

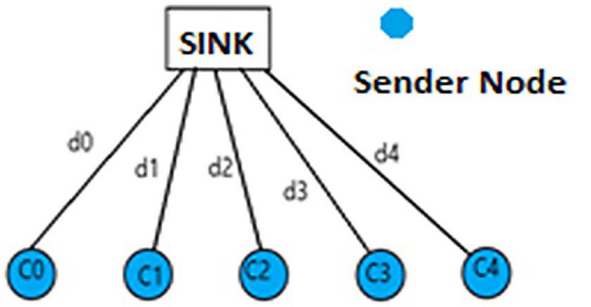

Fig. 2 Single hop Communication

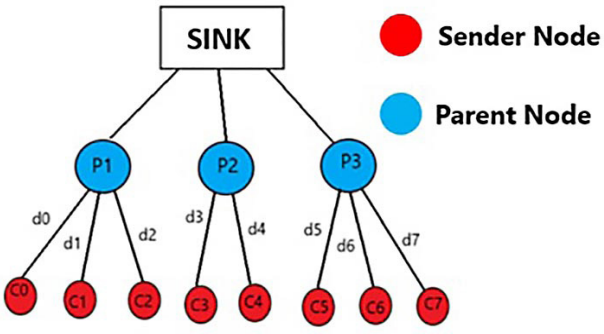

Fig. 3 Multihop Communication

Fig. 2 and Fig. 3 represent the single-hop and multi-hop communication respectively. In a single-hop communication, the packet from the source takes a single hop to reach its end-point address (sink). The number of hops depends upon the sender node to sink node distance and the energy it takes for every hop.

In multi-hop communication network, a packet has to pass through two or more nodes in to reach the end node (sink). Sensor networks are built of nodes ranging from hundreds to thousands of nodes that extends over huge distances. To interconnect nodes in large areas with minimal energy consumption, an approach is to use sensors as relays or intermediate nodes (parent node). Aptly said, nodes may not directly be connected to a destination address but use multiple hops to communicate their data which ultimately leads to efficient usage of battery [21]. In a WBAN, the distance between nodes is not too large but is constantly changing due to mobility of human body (Fig. 4).

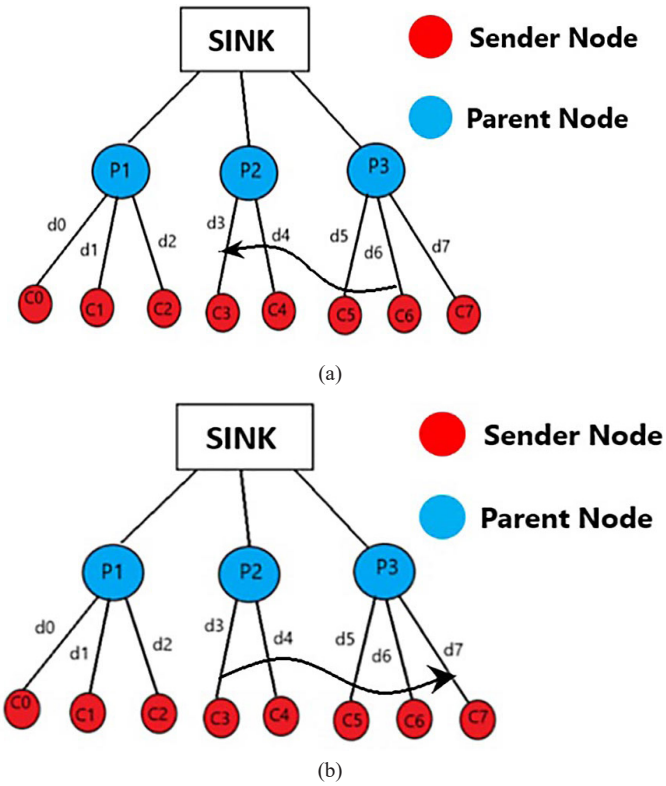

Fig. 4. Network Flow Tree Structure (a) Link Breakage (b) Link re-establishment

Human body cannot stay in a stationary condition for a long time and postures keep changing. In such a case, use of multi-hop communication is a better approach for an efficient data transmission. Several radio models have been proposed in the literature for energy consumption. The linear equation for first order radio model presented in [22] and is given by (1), (2) and (3).

$$E_{tx}(L,D) = E_{txelect}(L) + e_{amp}(L,D) \quad (1)$$

$$E_{tx}(L,D) = E_{txelect}.L + e_{amp}.L.D^2 \quad (2)$$

$$E_{rx}(L,D) = E_{rxelect}(L) = E_{rxelect}.L \quad (3)$$

Where E_{tx} is the energy used in transmission of data and E_{rx} is the energy used up while receiving of data. $E_{txelect}$, $E_{rxelect}$ are the energy necessary to run the transmitter and receiver electronic circuit respectively. e_{amp} is the energy required by amplifier circuit, L symbolizes size of data packet and D represents the distance between the transmitting and receiving node.

Energy model for target optimization requires development of equations for single-hop and multi-hop communication. Energy used up during single hop and multihop communication is given in [8] and shown by (4) and (5) respectively.

$$E_{tx} = (e_{amp} + E_{txelect}) * L * D^2 \tag{4}$$

$$E_{mh} = L * h[E_{tx} + (E_{da} + E_{rx}) * \frac{h-1}{h}] \tag{5}$$

Here, h denotes number of hops and E_{da} represents energy consumed in data aggregation. Rewrite the (5) with the help of (3) and (4), we have,

$$E_{mh} = \left[(e_{amp} + E_{txelect}) * h * (LD)^2\right) + (E_{da} + E_{rxelect}.L).L.(h-1)] \tag{6}$$

The Eq. (6) will serve as an objective function for optimization which depends upon *L* (packet size), *D* (node and sink distance) and *h* (hop count).

IV. Optimization

A. *Formulation*

Our aim is to optimize the energy consumed per hop in a Nanoscale WBAN multi-hop sensor communication by the objective function described in (6) via an optimizing algorithm.

B. *Optimization algorithms*

Optimization is a collection of mathematical/ computational principles and methods used for solving a problem where an objective function is either maximized or minimized by a systematic choice of input values from an allowed set which is constrained by some parameters [23]. Generally, optimization is finding "best fit" values of given objective function from definite and constrained input values. The choice of optimization technique depends on the problem to be addressed. Some optimization techniques that has been considered for the problem at hand are: genetic algorithm (GA), ant colony optimization (ACO) and particle swarm optimization (PSO).

B. *i. Genetic Algorithm (GA)*

GA is a meta-heuristic algorithm inspired from the natural selection and genetics [24]. In GA chromosomes are mutated, altered and estimated for the objective function in every iteration and those with better values are selected and reserved for succeeding iteration. The chromosomes for following iteration (child) are bred through crossover and mutation of those from the preceding iteration (parents). These newly bred chromosomes then act as parent chromosomes for succeeding iteration and the process carry on till specific stopping criterion is met [25]. A stopping criterion may be in the form of fixed number of generations reached or a solution is found.

The drawback of GA is that it gets confined in local minima or arbitrary points rather than global minimum. It cannot handle complexity in efficient manner and is better suited to discrete problems. Iba [26] presents the use of GA for reactive power optimization.

B. *ii. Ant Colony Optimization (ACO)*

ACO is a probabilistic technique based on population, where the artificial ants follow a procedure in search for food (optimized solution). A solution is created by iteratively summing the constituents considering (i) any experimental information about the problem being solved, and (ii) pheromone trails [25]. Pheromone trails are left by ants who tread the path earlier. These tracks disappear with time to assist search in new areas and avoid convergence to a local optimal solution [27].

The main drawback of this technique is its poor theoretical analysis, uncertain time of convergence and changes in probability distribution with iteration. ACO is applied for reactive power flow optimization in [28].

B. *iii. Particle Swarm Optimization (PSO)*

Particle swarm optimization is a computational algorithm developed by Kennedy, Eberhart and Shi. It is an optimization algorithm based on population (swarm) [29][30].The authors were motivated by the social behavior of animals like birds, fish, herds and ants and intended to simulate their behavior as a formalized representation of these organisms in a group. PSO has been used in various areas of optimization. PSO has gained importance for solving complex and hard optimization problems [31].

In PSO, swarm of particles move in N dimensional space to reach an optimal solution for a given objective function. The particles in this swarm have properties like current position of the particles and velocity of the particle. The motion of the particles is guided by their own known position in the space as well the entire population's best-known position. The particles adjust and update their position in such a way that an optimum or close to optimum solution is reached after multiple iterations [32].

PSO requires small number of parameters and lower number of iterations. Unlike GA, it tries to find global minimum and the variables in PSO can take any value based on their current position in particle space and corresponding velocity vector. PSO is faster in comparison to the other two algorithms and can be applied to problems that are noisy and dynamic [33].

For a continuous space which depends on the shape of the objective function and the number of constraints and their size, PSO is a better choice which comes as a conclusion of its speed, ability to converge and give accurate solution [34].

C. *Experiment*

The experiments have been performed in MATLAB 2019 running on windows 10 along with 8 GB of RAM.

PSO has been used to optimize the E_{mh} per hop for the given objective function in (6). Here D and L has been considered as the constrained parameters and E_{mh}, h, E_{tx} are free parameters. As in (4) it has been represented that variation of E_{tx} is between 10 nJ and 40 nJ, which is a permissible transmission energy range for Nano scale WBAN nodes. The results from (4) has been used in (6) and fed to PSO algorithm. The flow chart of PSO has been depicted in Fig. 5 and the parameters used for optimization are listed in Table II.

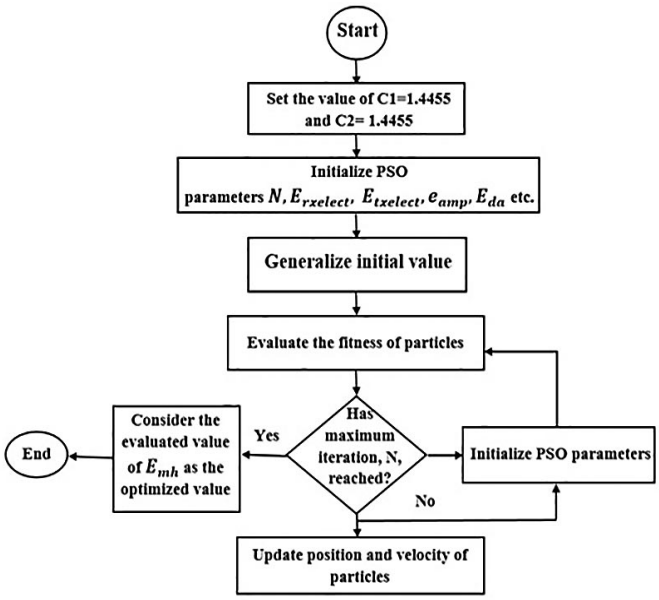

Fig. 5. Flow Chart of particle swarm optimization algorithm

TABLE II
PARAMETERS FOR PSO

Parameters	Value
Population Size	100
Final Weight, *w1*	0.4
Initial Weight, *w2*	0.9
Number of iterations, I_{tmax}	1000
Acceleration Constant (C_1, C_2)	1.4455, 1.4455
$E_{rxelect}$	36.1 nJ/bit
$E_{txelect}$	16.7 nJ/bit
e_{amp}	1.97 nJ/bit
E_{da}	5 nJ/bit

V. RESULTS

For the E_{tx} range from 10 nJ to 40 nJ, distance D obtained from (4) is 23 mm. For 1000 iterations performed in PSO, the optimized value of E_{mh} for varied hop count is best when L is 2000 bits. The values of parameters in optimization function (6) has been summed up in Table III.

TABLE III
OPTIMIZED PARAMETERS OF OBJECTIVE FUNCTION

Parameters	Value
$E_{rxelect}$	36. 1 nJ/bit
$E_{txelect}$	16.7 nJ/bit
e_{amp}	1.97 nJ/bit
E_{da}	5 nJ/bit
Packet size (L)	2000 bits
Distance	23 **mm

*nJ = nano Joule, mm = mili-meter

Table IV summarize the optimized and non-optimized values for energy consumption in the proposed model.

TABLE IV
OPTIMIZED ENERGY AND NON-OPTIMIZED ENERGY OBTAINED WITH RESPECT TO HOP COUNT

Hop Count	Non-Optimized Energy E_{mh} (per hop) (*J)	Optimized Energy E_{mh} (per hop)(*J)
2	0.289058022	0.072241515401
3	0.385358023	0.096298782984
4	0.433508023	0.10833397302
5	0.462398033	0.1154665893

*J = Joule

A comparative plot of non-optimized and optimized energy values for E_{mh}, E_{rx} and E_{tx} is shown in Figs. 6-8 respectively. In Table IV the value of optimized E_{mh} when packet size L is 2000 bits, and non-optimized E_{mh} when packet size is 4000 bits has been given. The table shows that optimized energy obtained for different hop count varies between 0.07224 J to 0.1154 J whereas non-optimized energy varies between 0.2890 J to 0.4624 J for hop count from 2 to 5 respectively.

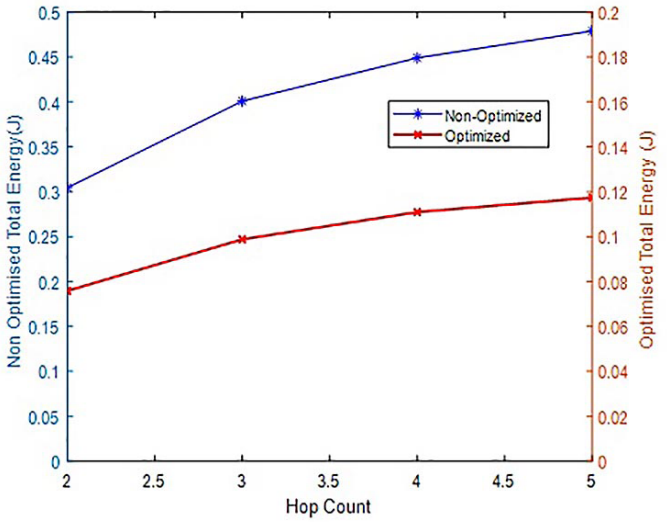

Fig. 6. Optimized E_{mh} (per hop) and Non-Optimized E_{mh} (per hop) with respect to Hop Count

TABLE V
OPTIMIZED ENERGY AND NON-OPTIMIZED RECEIVING ENERGY OBTAINED WITH RESPECT TO HOP COUNT

Hop Count	Non-Optimized Receiving Energy E_{rx} (1e-04 *J)	Optimized Receiving Energy E_{rx} (1e-04 J)
2	1.4444999856	0.72204997499
3	1.4444992220	0.72204998750
4	1.4444992220	0.72204999166
5	1.4444999966	0.72204999375

*J = Joule

The values of optimized energy and non-optimized energy were further used in (6) to optimize energy consumed in There is a significant decrease in the energy consumed per hop when the packet length is reduced to half its original length, as shown in Fig. 6. The optimization has been done with distance between nodes being comparable in case of optimized and non-optimized energy calculation .receiving data E_{rx} as shown in Table V. The optimized energy of receiving data is approximately 0.72204e-04 J with very minimal variation obtained with respect to hop count as compared to non-optimized receiving energy whose value obtained was approximately 1.4444e-05 J. The comparative plot is shown in Fig. 7. It is noticeable that the optimized receiving energy E_{rx} is significantly lower than non-optimized receiving energy.

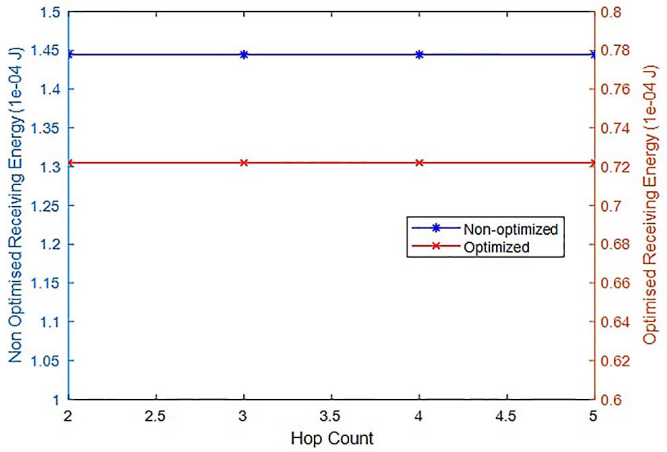

Fig. 7. Optimized Receiving energy and Non-optimized Receiving energy with respect to Hop Count

The values of optimized energy and non-optimized energy were further used in (6) to optimize transmitted energy E_{tx} as given in Table VI. The optimized transmission energy range is 1.5758e-08 J to 0.8529e-08 J as compared to non-optimized transmission energy whose range is 3.7006e-08 J to 3.5509e-08 J for the hop count of 2 to 5 respectively.

The comparison of the values is depicted in Fig. 8. It can be comprehended that the optimized transmission energy E_{tx} is significantly lower than non-optimized transmission energy. Table VII shows the percent difference of optimized values obtained E_{mh}/L (total energy consumed per bit length of data packet per hop), E_{tx}/L (energy used for transmission per bit length of data per hop) and E_{rx}/L (energy used for receiving per bit length of data per hop) against the respective non-optimized values.

TABLE VI
OPTIMIZED ENERGY AND NON-OPTIMIZED TRANSMISSION ENERGY OBTAINED WITH RESPECT TO HOP COUNT

Hop Count	Non-Optimized Transmission Energy E_{tx} (1e-08 J)	Optimized Transmission Energy E_{tx} (1e-08 J)
2	3.7006250000	1.5758950500
3	3.6224283333	0.93923250000
4	3.5756035000	0.94871342500
5	3.5505972000	0.85299650000

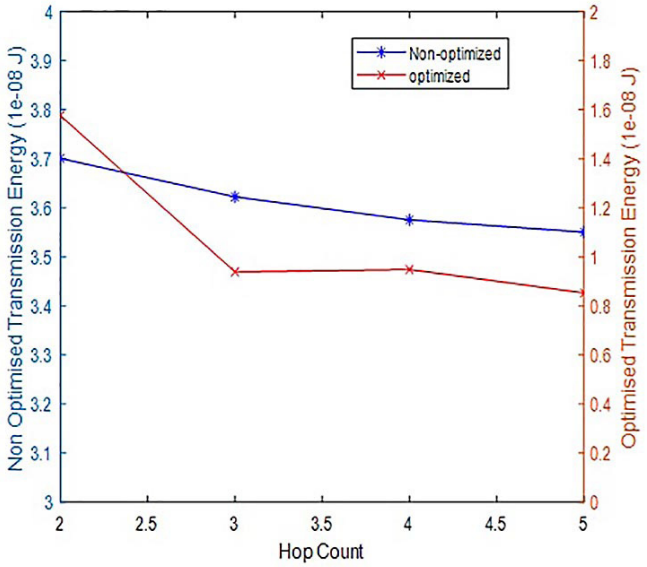

Fig. 8. Optimized Transmission energy and Non-optimized Transmission energy with respect to Hop Count

TABLE VII
PERCENTAGE DIFFERENCE IN NON-OPTIMIZED AND OPTIMIZED VALUES OBTAINED WITH RESPECT TO HOP COUNT

Hop Count	Percentage Difference in E_{mh} (%)	Percentage Difference in E_{tx} (%)	Percentage Difference in E_{rx} (%)
2	75.00795345	57.41543523	50.01384685
3	75.01056751	74.07174377	50.01381956
4	75.00992663	73.4670508	50.01384607
5	75.02874498	75.97597103	50.01384594

Fig. 9 shows the graphical representation of the percent optimization achieved. The total energy E_{mh}/L per hop is optimized by approximately 75% for hop count variation from 2 to 5, therefore signifying a similar level of optimization for each hop. E_{tx}/L per hop was optimized by approximately 57% to 76% for hop count from 2 to 5 respectively. E_{rx}/L per hop was optimized by approximately 50% for hop count from 2 to 5.

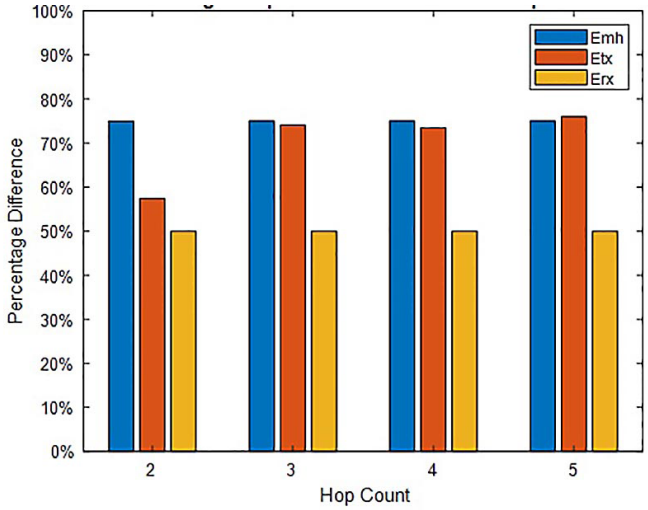

Fig. 9. Percentage difference in Non-Optimized and optimized values obtained with respect to Hop Count

VI. Conclusion

The energy efficiency of a WBAN network not only depends on the architecture and the routing protocol but also on node-to-node distance and length of the data packet to be transmitted. This paper has dealt with the energy efficient optimization problem with optimum node-to-node distance and length of packet to be transmitted. The optimization using PSO indicates that after reducing the packet length to 2000 bits and node-to-node distance to 23 mm, a significant decrease in energy consumption has been obtained. The total energy consumed per hop per bit length of data packet is optimized by approximately 75%. The energy consumed in transmitting data per hop per bit length of data packet is optimized by approximately 57% for 2 hops, 73% for 3 hops, 75% for 4 hops and 76% for 5 hops. The energy consumed per hop in receiving data per bit length of data packet is optimized by 50% for hop count from 2 to 5. This indicates that keeping nodes at a certain optimum distance and reducing the packet size of data to be transmitted results in reduction of energy consumed. The energy efficient transmission will prolong the lifetime of the sensors implanted in the human body which are otherwise impossible to replace.

In future works, other evaluation parameters can be used for optimizing energy in WBAN with inclusion of effect of path loss with every change in topology.

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Dual Notched-Band Crescent Moon Dielectric Resonator Antenna

Mohamed Debab, Amina Bendaoudi, and Zoubir Mahdjoub

***Abstract*— In this article, a dual-band notched ultra-wideband (UWB) dielectric resonator antenna is proposed. The antenna structure consists of Crescent Moon Dielectric Resonator (CMDR) fed by a stepped microstrip monopole printed antenna, partial ground plane, and an I-shaped stub. The Crescent Moon dielectric resonator is placed on the microstrip monopole printed antenna to achieve wide impedance bandwidth, and the I-shaped stub is utilized to improve impedance bandwidth for the WiMAX band. A comprehensive parametric study is carried out using HFSS software to achieve the optimum antenna performance and optimize the bandwidth of the proposed antenna. The entire band is useful with two filtered bands at 5.5 GHz and 6.8 GHz by the creation of notches. The band's rejection, WLAN band (5.2–5.7 GHz), and the downlink frequency band of ITU 7 GHz-band for satellite communication (6.5–7.3 GHz) is realized by inserting G-shaped and C-shaped slots in the ground. The simulation results demonstrate that the proposed CMDR antenna achieves satisfactory UWB performance, with an impedance bandwidth of around 88.7 %, covers the frequency band of 3.2 - 8.3 GHz, excluding a rejection band for the WLAN and ITU 7 GHz band. The CMDR is simulated using HFSS and CST high-frequency simulators.**

***Index Terms*— UWB, Crescent Moon Dielectric Resonator (CMDR), Dual band notched band, C-shaped slot.**

Original Research Paper
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I. Introduction

Initially, high permittivity dielectric resonators (DRs) are used as oscillators and filters in microwave circuits. In the last few decades, DR's are only used as energy storage devices rather than radiators. The idea of using DR as an antenna is widely accepted after work done on cylindrical dielectric resonator antenna (DRA) in 1983 [1]. Since dielectric resonator antennas have very low loss, higher efficiency without any conductor loss has ensued DRAs can be excited by different feeding mechanisms with various shapes [2]. Moreover, various types of feeding techniques were utilized to excite DRAs such as using a microstrip feed-line [3], [4] a rectangular waveguide [5], and a coaxial probe [6]. Several techniques have been reported to enhance the bandwidth of DRAs with the use of different configuration shapes, e.g., L-shaped, elliptical-shaped, T-shaped, and stair-shaped [7]–[11]. On the other hand, in the UWB operating frequency band, there exists interference from some narrowband, frequencies. Therefore, certain frequencies in the UWB range need to be rejected leading to a need for band-notched antennas. The main problem of band rejection design is the difficulty of controlling the bandwidth of the notched band in a limited antenna space. Recently, several UWB antennas with band-notched properties were presented where various methods have been used to achieve the band notching. Examples of approaches used are; L-shaped two slots and open-loop resonator [12], U-shaped slots [13], [14], E-shaped slot [15], inverted U-shaped slots and H-shaped slot [16], negative permittivity CSRR [17], and EBG structures [18].

In the present paper, a compact 25×25mm^2 CMDR antenna loaded on a 50Ω microstrip feed line is presented, the antenna can reject two narrow bands by creating narrow slots on the ground plane. The CMDR antenna achieves an impedance bandwidth of 3.2-8.3 GHz with a return loss $|S_{11}| \leq$ -10 dB and presents the decrement gain at 5.5 and 6.8 GHz. This manuscript contains four distinct sections. Section I is an introduction. Section II elaborates the effect geometry and position of the crescent moon dielectric resonator, the design principle with variable frequency band notch characteristics. The radiation pattern and simulation results of return loss with two simulators using CST and HFSS software are presented in Section III. Concluding remarks are presented in Section IV.

II. Antenna Design and Studies

Fig.1 shows the details of the CMDR antenna. The thin monopole antenna is printed on a Rogers RT5880 substrate 25×25 mm^2 whose thickness is 0.878mm, a relative dielectric constant of ε_r = 2.2, and loss tangent of 0.0009. The partial ground plane with a size of 25×8.4mm^2 is applied on the backside of the dielectric substrate. For impedance bandwidth improvement the crescent moon dielectric resonator and I-shaped tuning stub are added for the best matching of the monopole antenna. To create a crescent moon dielectric, the cylindrical dielectric resonator made of Silicon material (relative permittivity of 11.9, and loss tangent tan δ=0.015), with dimensions of R_{DR}=6mm, H_{DR}=14mm. A circular region is cut in the cy-

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lindrical dielectric resonator at position P_{DRC} (P_{RDCx}=9.5mm, P_{RDCy}=9.5mm) with a radius R_{RDC}=5mm. The key innovation in the proposed design is to use the G-shaped and C-shaped slots to achieve dual-notched band characteristics. The band-notched configurations are involved to produce the wanted stop bands with good frequency selectivity and suitable stop bandwidths to eliminate the interference at 5.2–5.7 GHz, and 6.7-7.3 GHz.

A commercial computer simulation tool High-Frequency Structure Simulator (HFSS), is used to design the antenna. The optimized dimensions are presented in Table I.

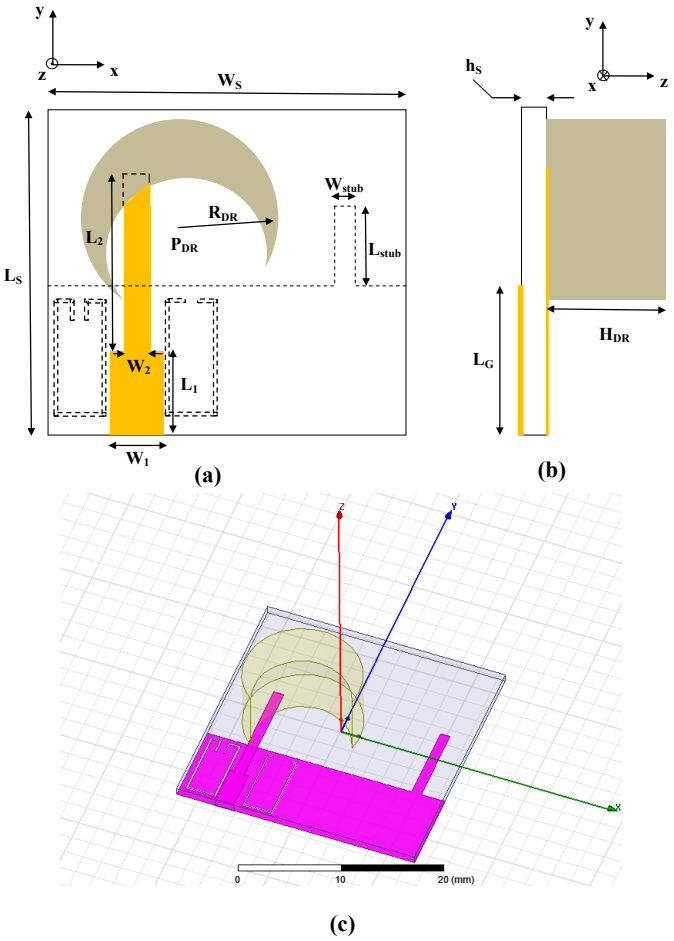

Fig. 1. Geometry of the CMDR antenna (unit: mm): (a) Top view, (b) Side view, (c) 3-D view.

TABLE I. The Parameters of the CMDR Antenna.

parameter	(mm)	parameter	(mm)
W_s	25	H_{DR}	14
L_s	25	P_{DRx}	8.5
h_s	0.878	P_{DRy}	12.5
W_1	2	R_{DRC}	5
L_1	4	P_{DRCx}	9.5
W_2	1	P_{DRCy}	9.5
L_2	11	L_{stub}	8
L_G	8.4	W_{stub}	1
R_{DR}	6		

A. Antenna Without Notches

The design procedure and the simulated reflection coefficients of the CMDR antenna are shown in Fig.2. To increase the bandwidth and move the lower band toward lower frequencies, a CMDR is loaded on the monopole. It can be seen that the monopole antenna loaded with the CMDR, achieves better impedance matching than the basic monopole antenna structure. But the antenna still presents some mismatches at low frequencies band (less than 3.6 GHz). So, to improve this impedance mismatching at low frequencies, an I-shaped tuning stub is added to the partial ground plane, as shown in Fig.2. When the CMDR and I-shaped tuning stub is present, the lower band shifts to 3.3 GHz and the antenna exhibits a sharp resonance dip of $|S_{11}|$ is -22.5dB at 5.2 GHz, and the height of the band shifts to 8.3 GHz. From the simulated results, it can be concluded that the CMDR antenna provides better reflection coefficient performance to cover the WiMAX band.

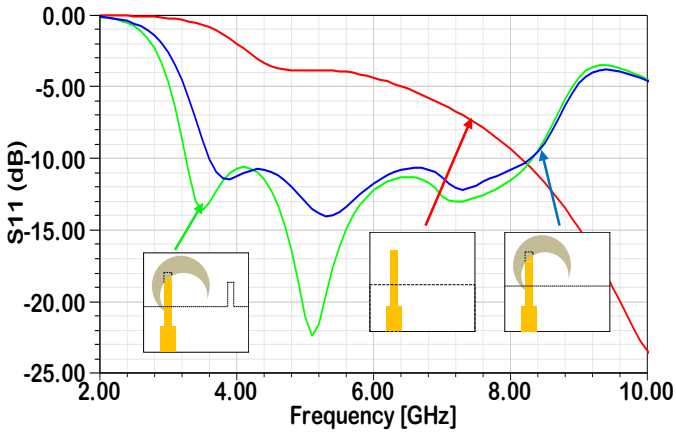

Fig. 2. Simulated $|S_{11}|$ for various antenna structures.

To accomplish an investigation of the characteristics of the CMDR antenna, to obtain the most effective antenna performance, a parametric study is achieved. The commercial software Ansoft HFSS is used for the parametric analysis. Important parameters of the CMDR antenna are investigated by changing each time a parameter while keeping other parameters unchanged.

Fig. 3 shows the effect of the radius R_{DRC} from 1 to 6 mm on antenna performance. It is clear that for $|S_{11}|$ less than -10 dB, the lower edge frequency of the bandwidth is about 3.2 GHz, and the height of the band shifts to 8.3 GHz. When R_{DRC}=5mm. The resulting antenna offers a broad impedance bandwidth of 88.7% for $|S_{11}|$ less than -10 dB.

The effect of the position, P_y on the reflection coefficient of the CMDR antenna is depicted in Fig. 4. From this figure, it is very clear that this parameter influences both the impedance matching and bandwidth of the CMDR antenna. As a result, the best impedance matching is achieved at P_y=12.5 mm.

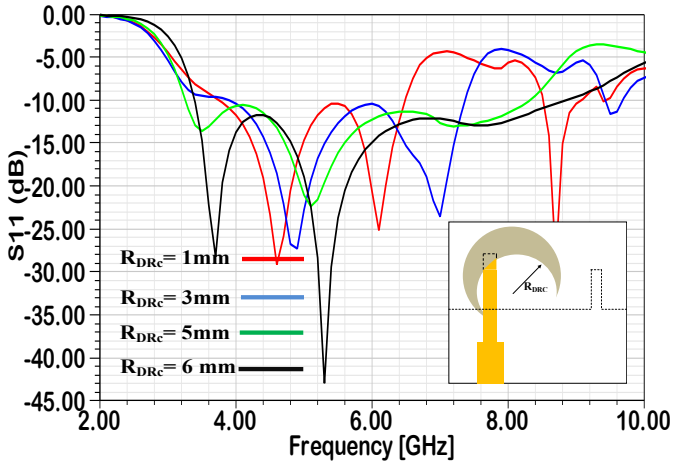

Fig. 3. Simulated $|S_{11}|$ parameters of the CMDR antenna with different values of radius RDRC.

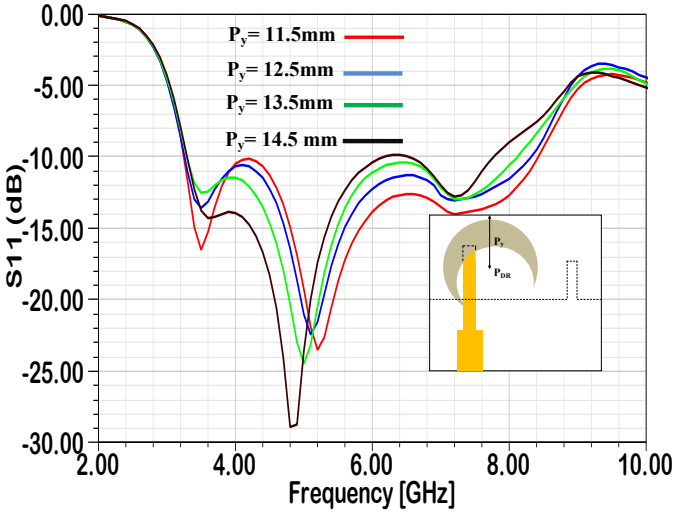

Fig. 4. Simulated $|S_{11}|$ parameters of the CMDR antenna with different positions P_y.

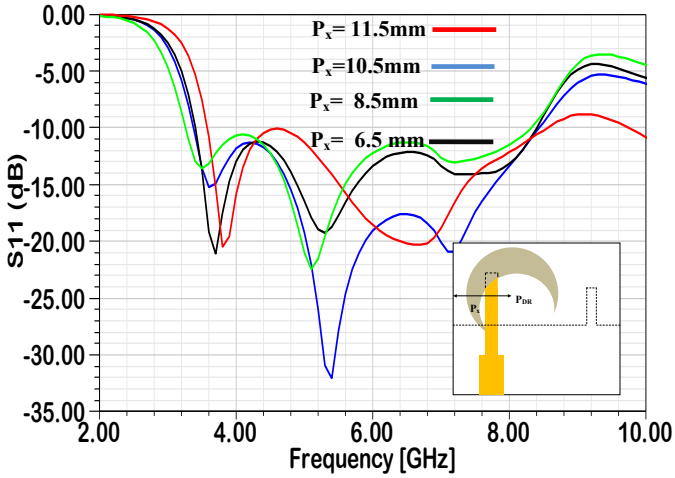

Fig. 5. Simulated $|S_{11}|$ parameters of the CMDR antenna with different positions P_x.

The position P_x has been optimized from 11.5 to 6.5mm to obtain the optimal impedance matching ($|S_{11}| \leq$ -10dB). The comparison of the reflection coefficient versus frequency plot for the different values of the position P_x has been depicted in Fig.5. It can be contemplated that for P_x=8.5 mm, the $|S_{11}|$ is $\leq$ -10dB at the frequency range of 3.2-8.3 GHz.

B. A Configuration of Uwb Antenna with Variable Frequency Band Notch Characteristic

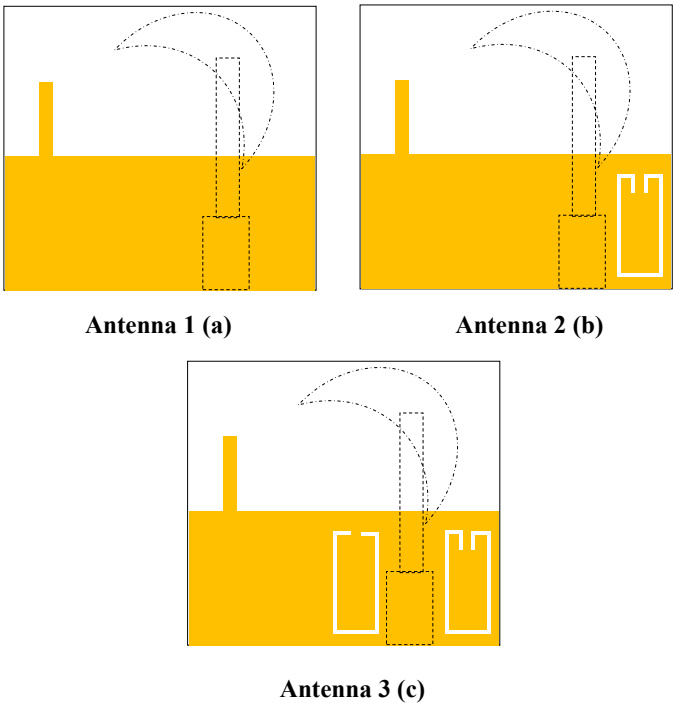

Fig. 6. Evolution of the CMDR antenna: (a) The CMDR antenna, (b) The CMDR antenna with etched G-shaped slot, (c) The CMDR antenna with etched G-shaped and C-shaped slots.

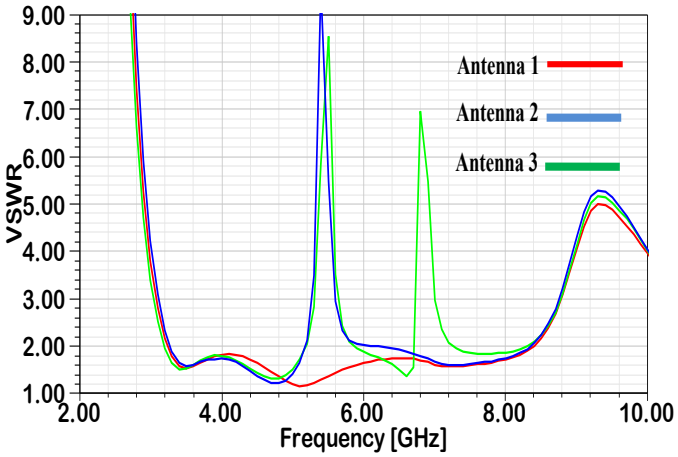

Fig. 7. Simulated *VSWR* of the CMDR antenna with and without slots.

Fig. 6 shows the evolution stages of the proposed design. The antenna is designed with a frequency range of 3.2-8.3 GHz as shown in Fig. 6 (a). By embedded a G-shaped slot on a

ground plane, the band stop function for WLAN is achieved as shown in Fig 6 (b). Dual-band stop characteristics for WLAN band and ITU 7 GHz by etching G-shaped slot and C-shaped slot on the ground plane. The proposed geometry is shown in Fig. 6 (c).

Fig.7 shows the VSWR curves of the evolution of the CMDR antenna. Antenna-2 anticipates the band notch characteristic only at the WLAN frequency band (5.2-5.7 GHz), whereas Antenna 3 shows the band notch characteristics at WLAN (5.2-5.7 GHz) and ITU 7 GHz band (6.7-7.3 GHz).

C. Notched Band for Wlan Band.

The G-shaped slot determines the notched band that rejects the WLAN band, and the designed central frequency of the notch band function is to adjust the length of the slot L_{WLAN} which cuts to approximately half wavelength. Fig. 8 depicts the geometry of the G-shaped slot to create band rejection to avoid the electromagnetic interference between nearby existing WLAN systems and UWB systems. The notched frequency can be assumed as [19]:

$$f_{notch} \approx \frac{c}{2\,L_{WLAN}\sqrt{\frac{\varepsilon_r+1}{2}}} \tag{1}$$

where L_{WLAN} is the total of the G-shaped, ε_r is the dielectric constant of the substrate, and c is the speed of the light. The total length of the slot L_{WLAN} is given by:

$$L_{WLAN} = 2(L_1 + L_2 + L_3) + L_4 = 22mm \tag{2}$$

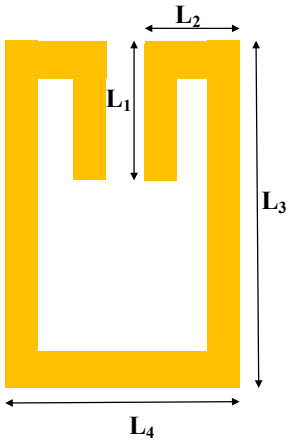

Fig. 8. G-shaped slot dimensions.

Fig. 9 shows the VSWR of the CMDR antenna after adding the C-shaped slot. As observed from the figure a notched band at about 5.5 GHz for the WLAN application is being created. Using equation (1) the theoretical predictions are compared to the total length simulation values L_{WLAN} in Table II. It is found that there are few differences between them.

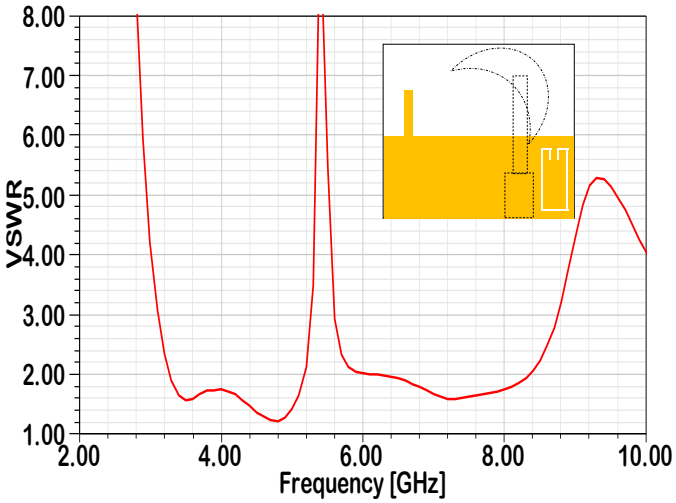

Fig. 9. Simulated *VSWR* of the CMDR antenna with band notch at *WLAN* band.

TABLE II. SIMULATIONS AGAINST THEORETICAL PREDICTION OF WLAN BAND-NOTCHED CMDR ANTENNA.

L_{WLAN} (mm)	Predicted (GHz)	Simulated (GHz)
21.2	5.59	5.70
22	5.39	5.50
22.8	5.20	5.30

D. Notched band for ITU 7 GHz Band

The notched band for ITU 7 GHz band is achieved by etching a C-shaped slot inside the ground plane. Fig.10 depicts the geometry of the C-shaped slot. The appropriate design of the band notch component obtained using the following relation [20]:

$$f_{notch} \approx \frac{c}{2\,L_{ITU}\sqrt{\frac{\varepsilon_r+1}{2}}} \tag{3}$$

Where L_{ITU} is the total length of the C-shaped slot, c is the speed of light, and ε_r is the dielectric permittivity of the substrate. The total length of the slot L_{ITU} is given by:

$$L_{ITU} = 2(L_1 + L_2) + L_3 = 17.8mm \tag{4}$$

From the illustrated Fig.11, a C-shaped slot is used to provide band stop function for ITU 7 GHz Band. It indicated the VSWR characteristics of the proposed geometry. It shows that the antenna provides a sufficiently wide impedance bandwidth (VSWR $\leq$ 2) of 5.1 GHz (3.2-8.3 GHz), and has a frequency notch of about 0.4 GHz (6.7-7.1 GHz) for band rejection of the ITU 7 GHz band. The L_{ITU} length simulation values are compared to the theoretical prediction in Table III. Note that the resonant frequency calculated using equation (3) is in good agreement with simulated notch frequency.

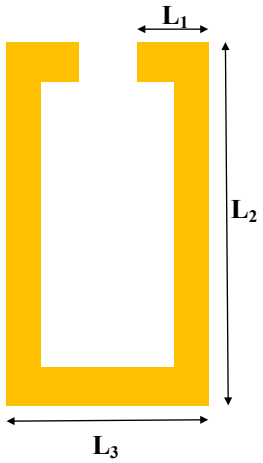

Fig. 10. C-shaped slot dimensions.

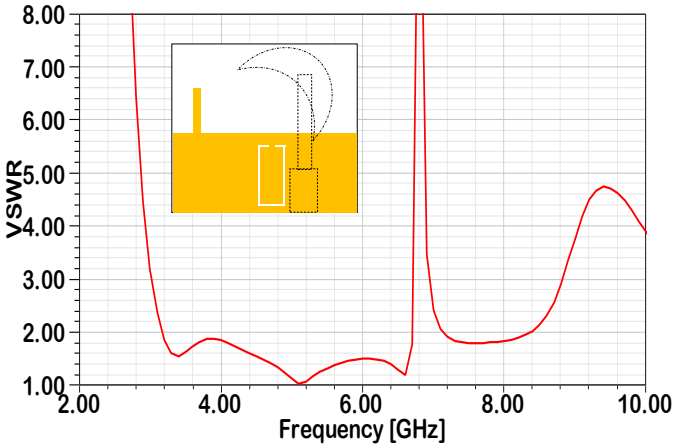

Fig. 11. Simulated *VSWR* of the CMDR antenna with band notch at *ITU* 7 GHz band.

TABLE III. Simulations against Theoretical Prediction of ITU 7 Ghz Band-Notched CMDR Antenna.

L_{ITU} (mm)	Predicted (GHz)	Simulated (GHz)
17.8	6.66	6.80
18.2	6.51	6.60
18.8	6.30	6.50

E. Parametric Study

To study the analysis and effect of various parameters on the bandwidth of notch bands, one parameter at a time is varied. The length L_{WLAN} and L_{ITU} of G-shaped and C-shaped slots are varied and its variation on VSWR is plotted in Fig. 12 and Fig. 13, respectively. The effect of the length L_{WLAN} is presented in Fig.12. The center frequency of the notched band decreases from 5.9 to 5.3 GHz as L_{WLAN} increases from 20.4 to 22.8mm. The figure indicates that any change in the length of the L_{WLAN} does not have any significant influence on the other notched frequency.

Fig.13 plots the VSWR of the CMDR antenna for different values of the length of the C-shaped slot L_{ITU}. It is observed that the center frequency of the band is shifted from 6.5 to 7.3 GHz as the length L_{ITU} changed from 18.8 to 17.2 mm, also observed that the variation in length L_{ITU} of C-shaped negligibly affects the bandwidth of other band notches.

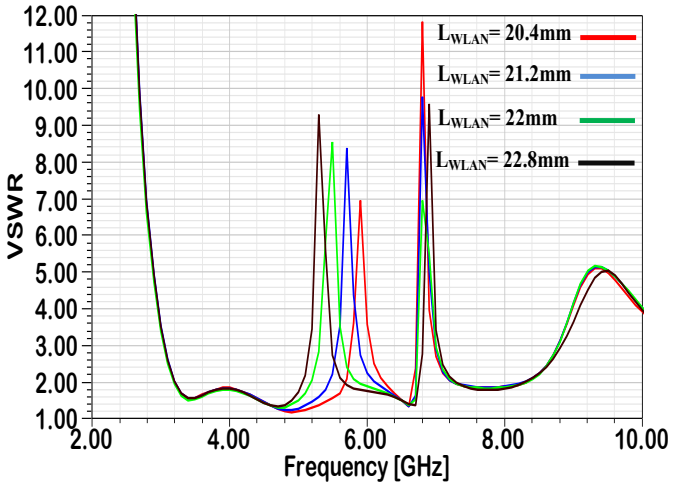

Fig. 12. Simulated *VSWR* of the CMDR antenna with different parameter *LWLAN*.

To understand the phenomena behind the notch band performance, the simulated surface current distribution of CMDR antenna at 5.5 and 6.8 GHz are shown in Fig. 14. It can be observed that at 5.5 GHz the surface current is confined in a G-shaped slot structure, whereas, at 6.8 GHz, the surface current is concentrated in a C-shaped slot. Thus, at these notch frequencies, the antenna will not radiate efficiently.

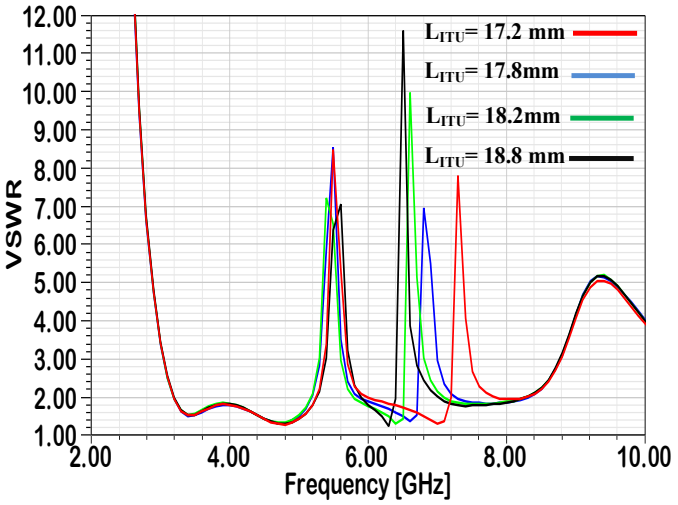

Fig. 13. Simulated VSWR of the CMDR antenna with different parameter *LITU*.

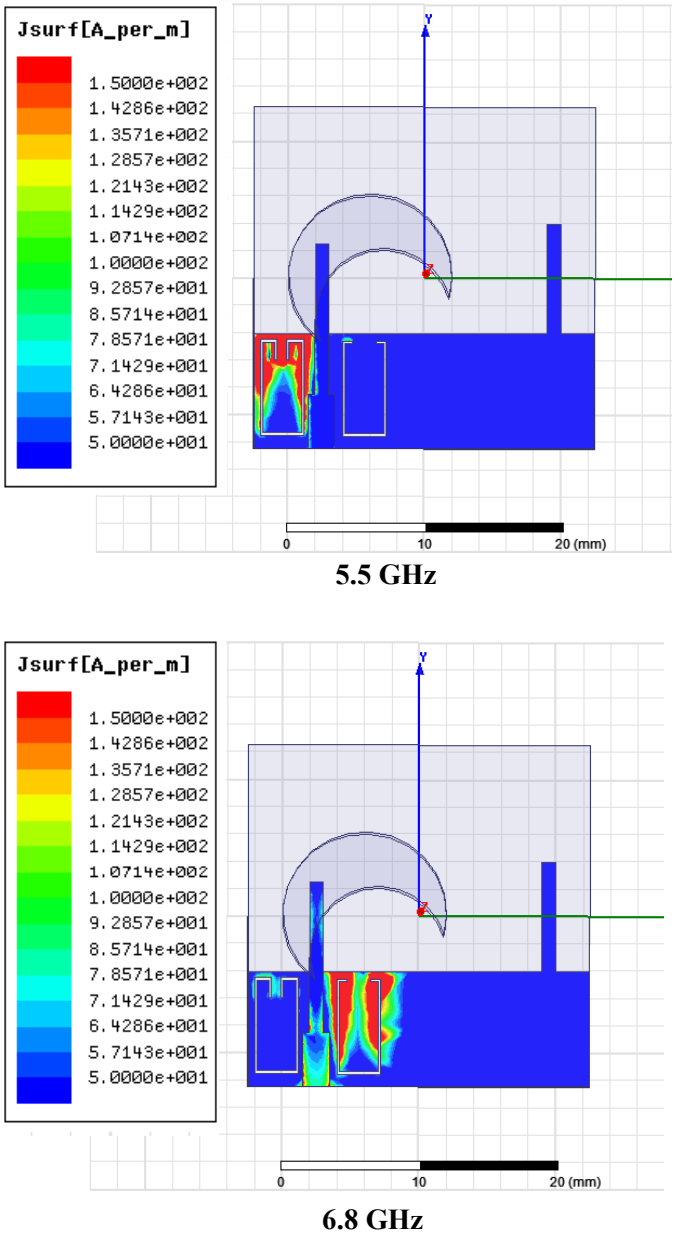

Fig. 14. Surface current distribution of the CMDR antenna at 5.5 and 6.8 GHz.

III. Results

To validate our use of design software HFSS, we designed and simulated the same structure as CST Microwave studio software whose numerical analysis is based on the method of the Finite Integration Technique (FIT). Fig.15 and 16 present the simulated VSWR and the reflection coefficient $|S_{11}|$ obtained by both simulation tools. This result shows a bandwidth of 5.1 GHz, covering frequencies from 3.2 to 8.3 GHz along with two notched bands of 0.5 GHz (5.2-5.7 GHz) and 0.6 GHz (6.7-7.3 GHz). The slight difference between the simulated results of CST and HFSS is due to the different numerical techniques employed by the two software.

The simulation results of radiation patterns at the following frequencies: 4 GHz, 6 GHz, and 8 GHz with two simulators HFSS and CST are shown in Fig. 17. The antenna exhibits an omnidirectional pattern at 4 GHz and it gets distorted and directional as the frequency of operating is increased. At 6 GHz, the radiation pattern is highly directive in the H plane and bidirectional in the E plane. As can be seen that a good agreement is achieved between the two simulators.

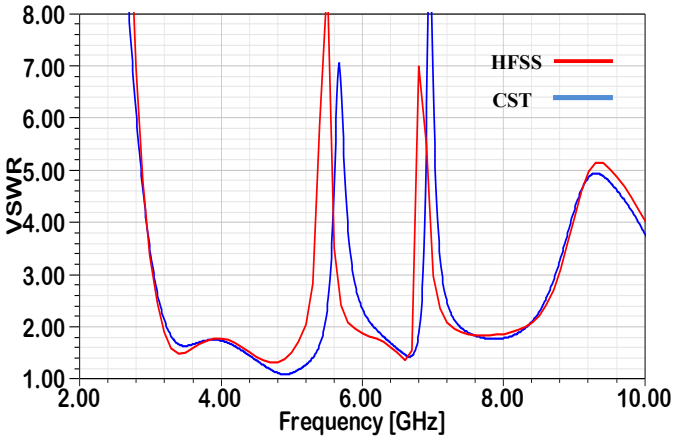

Fig. 15. Simulated *VSWR* of the CMDR antenna using HFSS and CST.

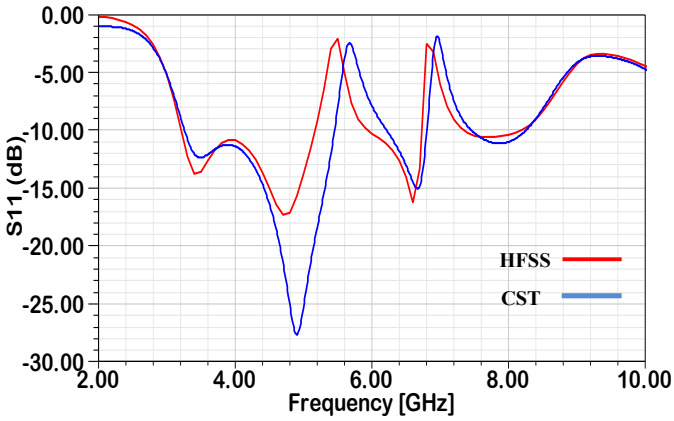

Fig. 16. Simulated $|S11|$ parameters of the CMDR antenna using HFSS and CST.

Fig.18 shows the simulated antenna gain response. The average gain for the dual band-notched antenna in the 3.2-8.3 GHz band is about 3.3dBi, however, at the notched bands 5.5 and 6.8 GHz, the antenna gain drops to about -5 and -2.5 dBi respectively.

The simulated radiation efficiency of the CMDR antenna with and without notch is depicted in Fig. 19. It is seen to have a sharp decrease across the notch band due to the existence of G-shaped and C-shaped slots on the ground plane. The radiation efficiency of the antenna the first notch (5.5 GHz) is 42% and a second notch (6.8 GHz) is 25%.

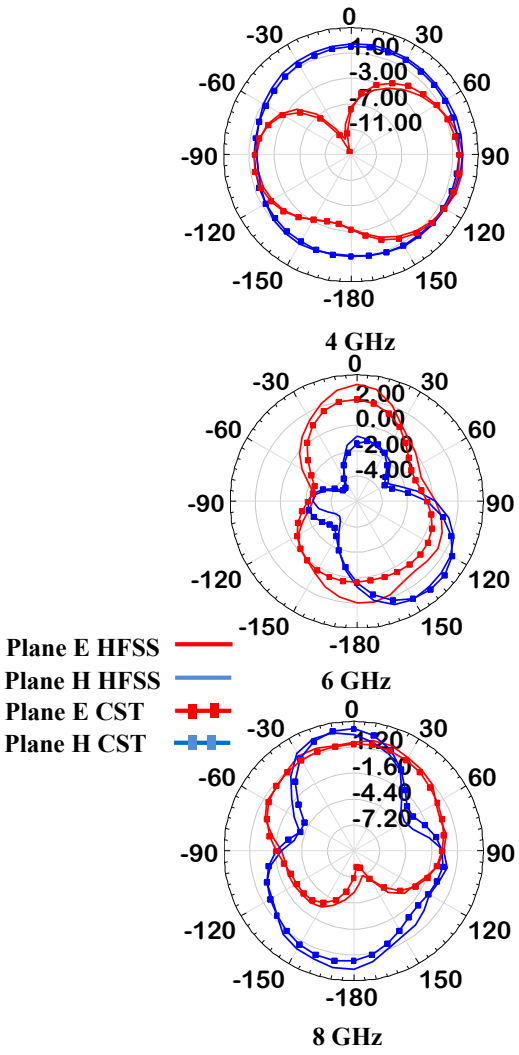

Fig. 17. CST and HFSS simulated directivity patterns in E (y-z) and H (x-z) planes for the CMDR antenna at 4, 6, and 8 GHz.

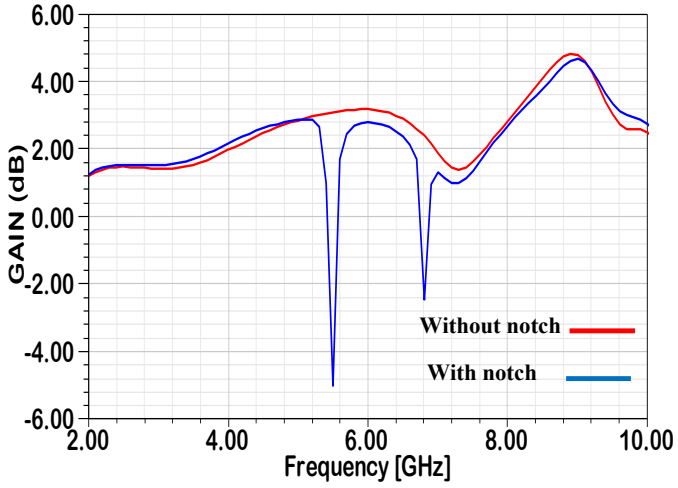

Fig. 18. Simulated peak gain with and without notch of the CMDR antenna.

The comparison of the CMDR antenna with existing antennas has been delineated in Table IV. It can be adorned from Table IV that the CMDR antenna is compact in size in juxtaposition to references [13], [21]–[25] except reference [26]. Though the size of the antenna designed in [26] is compact, this antenna has only a single band notch frequency. Based on the aforementioned discussion, it can be anticipated that the CMDR antenna is novel, compact in size with a new design, and useful for UWB applications with band notched characteristics at WLAN and the downlink frequency band of ITU 7 GHz.

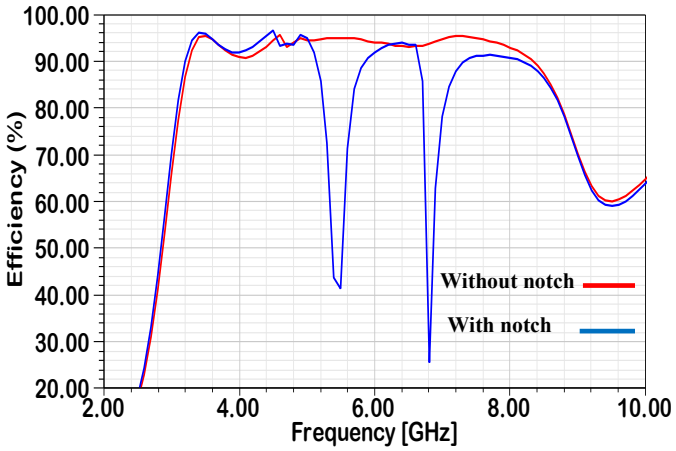

Fig.19. Simulated radiation efficiency with and without notch of the CMDR antenna.

IV. Conclusion

A dual-band notched dielectric resonator antenna is proposed. The UWB is obtained by incorporating a Crescent Moon Dielectric Resonator antenna excited by, a feed line. The I-shaped stub is utilized to improve impedance bandwidth for the WiMAX band. The final dimension of the CMDR antenna is 25×25×14mm^3. The first notch is realized at 5.5 GHz and the second notch is realized at 6.8 GHz by etching G-shaped and C-shaped slots on the ground plane, respectively. The notches prevent interference of 5.2-5.7 GHz (WLAN) and 6.7-7.3 GHz (ITU 7 GHz) communication bands.

The antenna offers UWB with 88.7% (3.2–8.3 GHz) of impedance bandwidth considering $|S_{11}| \leq$-10dB. The simulated results for the antenna VSWR and radiation patterns were provided with the use of HFSS software and were validated by using CST Microwave studio software. The slight difference between the simulated results is due to the different numerical techniques employed by the two software. The simplicity, compact size, low cost, and band rejection make this antenna suitable for UWB applications.

Acknowledgements

This work was supported by the directorate general for scientific research and technological development (DG-RSDT) of Algeria.

TABLE IV. Performance Comparison of the CMDR Antenna with Existing Dielectric Resonator Notched Antenna in Literature.

Ref	Type and shape of the Substrate	Size (mm^2)	VSWR band width range (GHz)	Type, height , and shape of the Dielectric Resonator	Efficiency (%) and Maximum gain at other UWB band (dB)	First rejected frequency band (GHz)	Peak gain of first rejected band (dB)	Second rejected frequency band (GHz)	Peak gain of second rejected band (dB)
[13]	FR4 ε_r=4.4 Rectangular shape	50 x 40	3.3-12	Dupont 943, ε_r=7.4 H_{DR}=6mm, Cylindrical shape	91, 7.6	WiMAX(3.4)	-0.6	---	---
[21]	RT 5880 ε_r=2.2 Rectangular shape	50 x 40	3.1-10.6	---, ε_r=10 H_{DR}=6mm, Rectangular shape	---, 4.5	WiMAX(3.4)	-1	WLAN (5.5)	-4
[22]	RT 3003 ε_r=3 Circular shape	π x $(120)^2$	2-10.7	Tmmi10, ε_r=10 H_{DR}=16.5mm, Inverted Conical shape	---, 8	WLAN(5.5)	-6.5	---	---
[23]	RT 6002 ε_r=2.94 Square shape	30 x30	3.5-10.5	---, ε_r=10.2 H_{DR}=5.08mm A-shape	---, 6	WLAN(5.08)	---	ITU-band Sat. Comm (6.2)	-3.5
[24]	Ground Square shape	90 x 90	3.6-12	Roger 6010, ε_r=10.2 H_{DR}=19mm, Rectangular shape	---, 8	WLAN(5.5)	-2	---	---
[25]	Ground Square shape	50 x 50	3.1-7.25	Roger 3006, ε_r=6.15 H_{DR}=6.5mm Rectangular shape	---, 6.8	WLAN(5.5)	-3	---	---
[26]	RT 3003 ε_r=3 Rectangular shape	11 x 23	3.1-15.25	Eccostock Hik, ε_r= 20 H_{DR}=2mm, S-shape	95, 4.8	WLAN(5.5)	0.9	---	---
Our work	RT 5880 ε_r=2.2 Square shape	25 x 25	3.2-8.3	Silicon, ε_r=11.9 H_{DR}=14mm, Crescent Moon shape	96, 3.6	WLAN(5.5)	-5	ITU-band Sat. Comm (6.8)	-2.5

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On The Implementation of Densely Packed Decimal Number System based Adder: Prospects and Challenges

Srikant Kumar Beura, Rekib Uddin Ahmed, Bishnulatpam Pushpa Devi, and Prabir Saha

***Abstract*—Decimal digit number computation, through bit compression methodology, offers space and time saving, which can be incurred by the Chen-Ho and Densely Packed Decimal (DPD) coding techniques. Such coding techniques have a property of bit compression, like, three decimal digits can be represented by 10 bits instead of 12 bits in binary coded decimal (BCD) format. The compression has been obtained through the elimination of the redundant 0's from BCD representation. This manuscript reports the pros and cons of the techniques mentioned above. The logic level functionalities have been examined through MATLAB, whereas circuit simulation has been verified through Cadence Spectre. Performance parameters (such as delay, power consumption) have been evaluated through CMOS gpdk45 nm technology. Furthermore, the best design has been chosen from them, and the decimal adder design technique has been incorporated in this paper.**

***Index Terms*—Chen-Ho coding, DPDcoding, Power, Delay, Decimaladder.**

Original Research Paper
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I. Introduction

Decimal arithmetic has been highly emphasized lately due to the increasing role of commercial, financial, and internet-based applications. The human interpretation of numbers in the decimal system is considerably more accessible than the binary system. Therefore, a decimal-based implementation approaches like fractions becomes more relevant from its counter-part, i.e., the binary system, which incurs recurring infinity bits [1]. Thereby, it is expected that inputs and outputs of the decimal notation from the machine also need to be decimal. The cost of hardware, which is the paramount concern for the digital arena, is increased due to its conversion, programming, and troubleshooting. Consequently, it seems more logical to implement decimal arithmetic in machines instead of forcing users to think in binary mode [2].

Decimal to binary conversion and vice versa is the prime requirement while adding two decimal numbers using binary adders. Meanwhile, the hardware required for this purpose increases with an increase in the decimal number value. This increase in hardware is the continuous division (Double dabble method) and multiplication operations performed in decimal to binary and binary to decimal conversions. Furthermore, the conversion of fractional decimal numbers into binary causes recurring infinity bits. Thereby, the converted decimal fraction number becomes incorrect and causes approximate errors [17]. Moreover, it affects the overall speed of operation of the addition process.

For decimal computation, each digit individually can be represented in binary coded decimal (BCD), and each of them can also be represented into four binary bits. Also, the same can be expressed compactly, like Chen–Ho [2] and Densely Packed Decimal (DPD) [1] coding,which are more lucrative in certain circumstances.

In 1975 Chen and Ho proposed an effective encoding technique (Chen-Ho encoding) to represent decimal data [2], which usually compresses three decimal digits into 10 bits rather than 12 bits. By considering the Huffman Code [3], various digit combinations have been formed using leading indicator bits. The Huffman code helps to determine the smaller (0 to 7) and larger (8, 9) digits present in a multi-digit decimal number. Furthermore, Chen–Ho encoding gives 17% more compact encoding than BCD with little waste. Simple Boolean operations are used for conversion or re-conversion. Floating-point decimal numbers can also be encoded in binary register using Chen-Ho encoding [4].

Another coding technique, namely DPD methodology [1], permits subjective length decimal numbers to be coded efficiently. DPD also performs compression of the three decimal digits into 10-bit instead of 12. This coding technique has also been based on Huffman coding, similar to the previously mentioned Chen–Ho encoding. Analogous to BCD encoding, DPD encoding allows all smaller and larger bits to be right-aligned. In contrast, Chen-Ho encoding follows the BCD pattern only

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for smaller digits (0 to 7), whereas for higher digits (8,9), it gives more weightage to the MSB. On the otherhand, the Chen-Ho algorithm requires completely different coding for single, double, and three decimal digits. However, the same algorithm is applicable for DPD to represent single, double, and three decimal digits with zero paddings on the left side only.

Moreover, computational circuitry, like the addition of decimal numbers, non-speculative adder takes less delay and consume nearly the same space than speculative adders [5]. A different non-speculative adder has been proposed by Lin et al. [6], where binary carry-save adder (CSA) is used on BCD input along with a correction module. Svoboda [7] has proposed a signed digit decimal adder considering the digit set [-6, 6]. In [7], each decimal digit (x) is multiplied by 3, and the multiplication result is stored in 5-bits, where significant overhead is required for the signed digit code conversion. Furthermore, researchers have proposed several decimal adders with precision in various literatures [8]–[14]. The adders offered by Bohlender et al. [9] and Cohen et al. [10] have quite long latencies while producing each result. A speculative signed-digit adder was proposed by Moskal et al. [12], where both the input operands are represented as sign-digit numbers.The operand is selected as apositive 4-bit vector and anegative 4-bit vector. The implementation technique is good enough with the penalty of algorithmic complexity. In [13]-[14], researchers have proposed an adder/subtractor module for signed magnitude format, with the scarification of other two significant VLSI aspects, i.e., delay and power consumption.

In this paper, the design technique of Chen-Ho and DPD coding has been addressed as a function of bit-positioning. Both coding techniques were simulated in MATLAB to analyze each code's bit-positioning and, later on, simulated in Cadence Spectre to compare the delay and average power consumption. Furthermore, a 3-digit decimal adder using the DPD coding technique has been proposed in this paper. The proposed decimal adder is compared with the existing designs [13]-[14], [16]-[17] as a function of the VLSI performance parameters such as delay and average power using gpdk45 nm technology. For the validation of the proposed decimal adder's exactness, image addition has been carried out and compared.

The manuscript is organized as follows: Section II providing pieces of information about some existing designs; Section III gives the brief logic behind the design of both the coding techniques; Section IV shows the comparative analysis of both the coding techniques as a function of power and delay; Section V demonstrates the implementation of the proposed DPD based decimal adder; Section VI shows the observations between proposed and existing adders; Section VII belongs to the application: image addition, followed by the conclusion (Section VII).

II. Related Work

In digital systems, the decimal numbers are usually encoded in BCD for arithmetic operations. The BCD adder takes two BCD digits as an input and provides the addition result, which is also in BCD [15].

The architecture of the conventional BCD adder has been shown in Fig. 1. There are two decimal digits, namely Aand B. The addition operation has been performed using binary adders, e.g., ripple carry adder (RCA) or carry look-ahead adder (CLA). The summation result has to pass through another stage where the correction needs to be completed. The intermediate summation result is denoted by *S3,S2,S1*,and *S0*. The *Carry-out* and final summation result (*Sum3-Sum0*) have been generated by adding '0110' to the intermediate summation result.

From Fig. 1, it has been observed that the delay of reported architecture is directly proportional to the digit width of decimal input. There are a few short-comings of the BCD adder, which are summarized below.

- For the generation of early carry, the BCD adder needs extra circuits. Moreover, ~20% more circuitry is required for the BCD addition than conventional binary addition.
- Usually, BCD representation (4-bits per digit) of decimal digits increases the storage space by ~20% than the standard binary encoding, which results in storage overhead.
- It has been observed that, in any operation, the practical implementation of BCD is much slower than the binary representation.

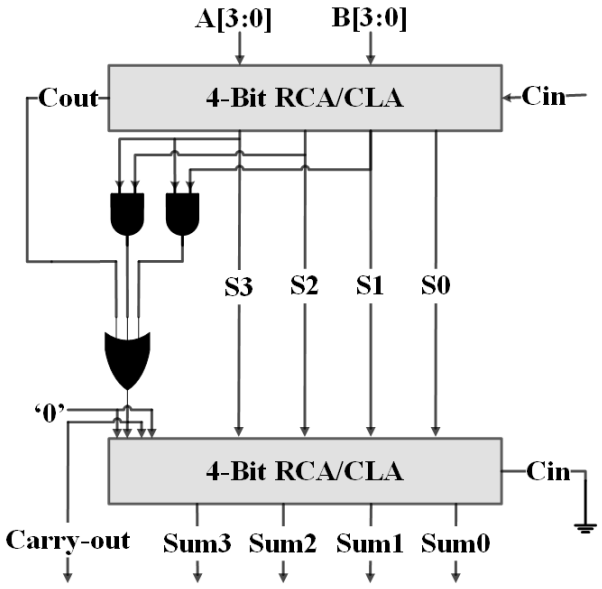

Fig. 1. 1-digit BCD adder [15]

In [16], the authors have proposed a fast BCD addition method known as fast decimal adders. The fast decimal adder's architecture also consists of three stages which is shown in Fig. 2. This adds two decimal numbers having three-digit each. Therefore, in binary, the inputs are *A*[11:0], *B*[11:0], and the *Cin*. In stage 1, both decimal digits are (each represented by 12-bits in binary) added together using CLA to obtain binary *Sum*[11:0] along with generate and propagate signals. *DPi* is the digit propagate signal, whereas *DGi* is the Digit Generate signal. *DPi* and *DGi* have been used to check whether the binary sums are equal to 9 and bigger than 9, respectively. The boolean expressions to represent *DPi* and *DGi* are provided

in eqn. (2), (3). In stage 2, in order to calculate the real decimal carries *Carry*[i] (as shown in eqn. 1), *DPi* and *DGi* signals have been considered as an input to the Carry network, which is made up of a parallel-prefix computation unit. Lastly, in stage 3, the summation of the correction values and the binary sums produced by stage 1 has been carried out to generate the final summation result [12:0].

$$Carry[i] = DGi + DPi \cdot Carry[i - 1] \quad (1)$$

$$DGi = Cout + (S[i + 3].(S[i + 2] + S[i + 1])) \quad (2)$$

$$DPi = S[i + 3] .S[i + 1]) \quad (3)$$

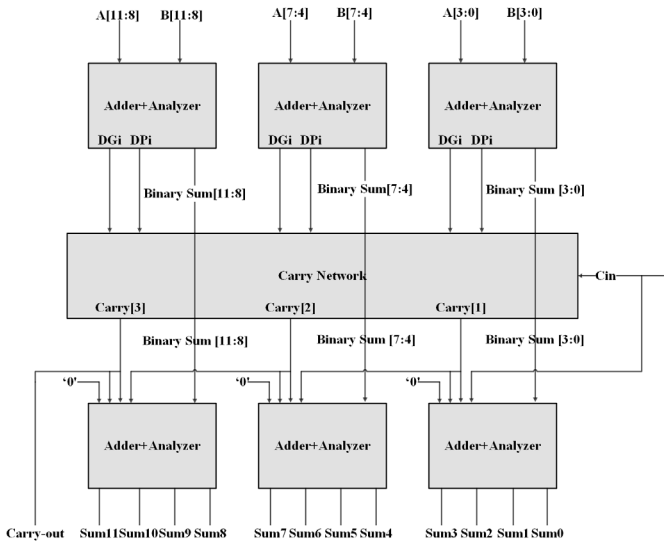

Fig. 2. Reduced delay BCD adder [16]

Researchers in [17] have proposed a similar decimal adder as in [16] with some significant modifications. This decimal adder [17] has been adding three decimal numbers of 4-digit each simultaneously. In stage1, binary converted decimal digits are fed to the CSA+PG unit. This CSA+PG unit is generating *DPi* and *DGi* signals along with Sum and Carry outputs. The decimal carries are computed in the 2nd stage with the help of carry network. The sums are calculated in the last stage by using carry-save adders (CSA) plus 4-bit carry-lookahead adders (CLA) which are adding the digit sums and carries with correction values.

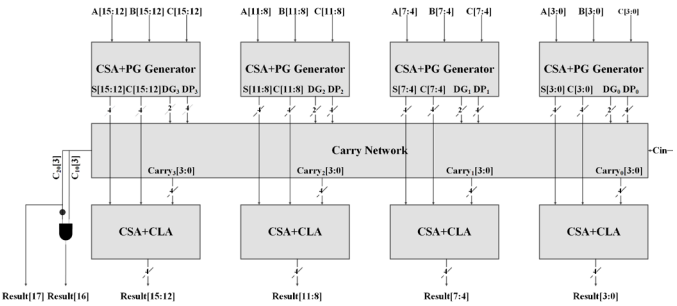

Fig. 3. Area Efficient Decimal Adder [17]

III. Description of Chen-Ho and DPD Coding Techniques

A. Chen-Ho Encoding

BCD encoding technique required four bits to represent each decimal digit. For example, if A is denoted as a single-digit decimal number, then the four-bits are needed to represent Ain BCD, i.e., *abcd*, such that $A = 8a + 4b + 2c + d$. Similarly, two decimal digits *A,B* can be represented as *abcd efgh* and three decimal digits *A,B,C* can be described as *abcd efgh ijkl* and so on.

The representation of each decimal digit as 4-bits conserve extra space, as four bits indicate 16 states (0 to 15),preferably 10 (0 to 9). Thereby, the relative inefficiency of BCD encoding with the help of binary notation (r) [2], i.e., $r = 4 \log 2/\log 10 = 1.204$. Therefore, the binary representation is saving 20.4% of space as compared to BCD.

To represent small decimal digits (0-7) in BCD format requires 4-bits (*abcd*), whereas these can be expressed in 3-bit (*bcd*) only. For the encoding of larger digits (8, 9), BCD needs four digits (*abcd*). However, for larger digits, a is always logic '1' and d is logic '0' for 8 and logic '1' for 9. Furthermore, bc is still the logic '0' for larger digits. Therefore, in Chen-Ho encoding, bc has been omitted for larger digits. By merely discarding the repetitive 0 bits in a BCD message, a consolidated code is obtained.

Chen-Ho proposed an efficient encoding by using the 'indicator field' and 'detailed field'. The role of this indicator bit is to specify the occurrence and the position of the larger digit. In combination with the indicator bit, the detailed field gives the larger decimal digit's actual value.

The 3-digit decimal number mapping issue can be resolved with Huffman encoding [3], which has been used in Chen-Ho encoding. The 3-digit decimal number in BCD is represented by 12 bits (*abcd efgh ijkl*). Three bits, namely (*a,e,i*), have been used as indicator bits. Therefore four cases may arise depending upon the smaller (0 to 7) and larger (8,9) bit combination, which are provided in Table I.

Table I
Logic Used for Chen-Ho Encoding

Case 1	When all 3-digits decimal numbers are small (0-7), the possibility of occurrence is 51.2%, encoded by (0).
Case 2	If any 1-digit decimal number is large (8,9), then the possibility of occurrence is 38.4%, encoded by (100, 101, 110).
Case 3	If 2-digits decimal numbers are large, then the possibility of occurrence is 9.6%, encoded by (11100, 11101, 11110)
Case 4	If all three decimal digits are large, then the possibility of occurrence is 0.8%, encoded by (11111).

The representation of 3-digit decimal numbers (*abcd efgh ijkl*) in the 10-bit binary was given (*pqrstuvwxy*). From the resulting bits (*pqrstuvwxy*), (*s,v,y*) is always standing with (*d,h,l*) of the BCD digits. Table II shows the compression of 3-digit decimal numbers into 10-bit.

Furthermore, Chen-Ho demonstrated that no arithmetic operation had been implemented; instead, only shift, deletion, and insertion is used. The Boolean algebra used for encoding of 12-bit into 10-bit binary and decoding is provided in Tables III and IV.

Table II
The Compression Algorithm of 12-bits Into 10-Bits (Chen-Ho)

a	e	i	p	q	r	s	t	u	v	w	x	y
0	0	0	0	b	c	d	f	g	h	j	k	l
1	0	0	1	0	0	d	f	g	h	j	k	l
0	1	0	1	0	1	d	b	c	h	j	k	l
0	0	1	1	1	0	d	f	g	h	b	c	l
0	1	1	1	1	1	d	0	0	h	b	c	l
1	0	1	1	1	1	d	0	1	h	f	g	l
1	1	0	1	1	1	d	1	0	h	j	k	l
1	1	1	1	1	1	d	1	1	h	0	0	l

Table III
Boolean Algebra for The Compression of 12-Bits Into 10-Bits

Compression into 10 Bits	
p	$a + e + i$
q	$b\,\bar{e} + i + a\,e$
r	$c\bar{\imath} + e + ai$
s	d
t	$ae + f\,(a + \bar{\imath}\,) + be\bar{\imath}$
u	$ai + g\bar{e} + ce\bar{\imath}$
v	h
w	$j + bi + fai$
x	$k + ci + gai$
y	l

Table IV
Boolean Algebra for The Expansion of 10-Bits into 12-bits

Expansion into 12 Bits	
a	$p\bar{q}\bar{r} + pqr(t + u)$
b	$q\bar{p} + tp\bar{q}r + wq(\bar{r} + \bar{t}\bar{u})$
c	$r(\bar{p} + \bar{q}u) + xpq(\bar{r} + \bar{t}\bar{u})$
d	s
e	$pr(\bar{q} + \bar{u} + t)$
f	$t(\bar{p} + \bar{r}\,) + pqr\bar{t}uw$
g	$u(\bar{p} + \bar{r}\,) + pqr\bar{t}ux$
h	v
i	$pq(\bar{r} + \bar{t} + u)$
j	$w(\bar{p} + \bar{q} + rt)$
k	$x(\bar{p} + \bar{q} + rt)$
l	y

B. Improvement on Chen-Ho Encoding

The Chen-Ho encoding works effectively when it deals with a 3-digit decimal number. Meanwhile, if the number of decimal digits is other than 3-digit (either one or two-digit), then Chen-Ho encoding does not work; hence this encoding needs to be redesigned. These are some points that need improvement in Chen-Ho encoding:

1. Chen–Ho encoding requires different coding techniques for 2-digits and 3-digits fields.
2. Chen–Ho encoding represents 12-bit into 10-bit binary. Therefore, it is always mandatory to use three decimal digits for the conversation.
3. Chen–Ho encoding follows the BCD pattern for encoding the decimal numbers 0 to 7, whereas for the encoding of decimal numbers 8 and 9, it gives more weightage to the most significant bits (MSB).

DPD encoding provides enrichment on Chen-Ho encoding. The DPD encoding utilizes a corresponding Huffman code over Chen-Ho, yet with a different way of representation of bits, which has considerable advantages:

1. The Boolean logic used for the compression of a 3-digit decimal number can be used to compress 1-digit or 2-digit decimal numbers. Thereby, any decimal number up to 3-digit can be encoded efficiently.
2. DPD offers the same bit positioning of the encoded bit as in BCD (all decimal numbers from0 to 79), which can be achieved by adequately positioning and choosing the indicator bit.

Table V illustrates the comparison between different encoding techniques. It shows the coding style of BCD,Chen-Ho, and DPD for a particular decimal number in a different position.

Table V
Comparison of Different Encodings

Decimal	Conversion to Binary		
	BCD	***Chen-Ho***	***DPD***
7	0000 0000 0111	000 000 0111	000 000 0111
9	0000 0000 1001	110 000 0001	000 000 1001
77	0000 0111 0111	000 011 1111	000 111 0111
99	0000 1001 1001	111 000 1001	000 101 1111
777	0111 0111 0111	011 111 1111	111 111 0111
999	1001 1001 1001	111 111 1001	001 111 1111

It can be observed from Table V that for the first three decimal numbers, BCD and DPD have similar coding with single and double-digit decimal numbers using only 4 and 7-bits, respectively. In contrast, Chen-Ho encoding has been utilizing all 10-bits for the representation of single and double-digit decimals. Therefore, Chen-Ho encoding consumes more memory than DPD encoding.

C. DPD Encoding

DPD encoding has been introduced as an improved encoding technique for smaller digits (0 to 7) and larger digits (8, 9) over Chen-Ho encoding. Moreover, due to the change of encoding logic, DPD provides a significant improvement in bit positioning. The 3-digit decimal number consists of either smaller or larger digits or a combination of smaller and larger digits. Therefore, four possible combinations are described in Table VI.

Table VI
Logic Used for DPD Encoding

Case 1	Let all 3-digits are small It requires 9-bits to represent three decimal digits, leaving 1-bit as an indicator bit.
Case 2	Let anyone digit is large It needs 7-bits to represent three decimal digits, leaving 3-bits for the indication (to know the larger digit's exact value and positioning).
Case 3	Let any two digits are large Now 5-bits needed for three-digit decimal representation, leaving 5-bits for indication.
Case 4	Let all three digits are large Finally, 3-bits are required for three-digit decimal number representation, leaving 7 bits for indication, whereas 5-bits are enough.

a. *Compression of 3-digit decimal (12 bits) into 10 bits using DPD:*

The compression of a 3-digit decimal number (*abcd efgh ijkm*) into 10 bit (*pqr stu v wx y*) can be done using the mapping technique, as depicted in Table VII.

Table VII
Compression of 3-Digit Decimal Number (12-Bits) Into DPD (10 Bits)

a	e	i	p	q	r	s	t	u	v	w	x	y
0	0	0	b	c	d	f	g	h	0	j	k	m
0	0	1	b	c	d	f	g	h	1	0	0	m
0	1	0	b	c	d	j	k	h	1	0	1	m
0	1	1	b	c	d	1	0	h	1	1	1	m
1	0	0	j	k	d	f	g	h	1	1	0	m
1	0	1	f	g	d	0	1	h	1	1	1	m
1	1	0	j	k	d	0	0	h	1	1	1	m
1	1	1	0	0	d	1	1	h	1	1	1	m

In this compression algorithm, 'v' has been regarded as the indicator bit. If the 3-digit decimal number contains at least one larger number (8, 9), then 'v' is considered 1, and if the three-digit decimal number contains only smaller numbers (0-7), then 'v' is denoted by 0. For example, if the 3-digit decimal number is 786, it will be represented as 0111 1000 0110. Now the value of a=0, e=1, and i=0. Therefore, it will follow the compression technique, as shown in the fourth row of Table VII. The value of 'v' is now 1, and w, x is denoted by 0 and 1, respectively. The remaining 7-bits are mapped from the input bit pattern by following Table V, and the resulting compressed encoding is given by 111 110 1010.

b. *Expansion of 10 bits into 3-digit decimal (12 bits) using DPD:*

This operation needs to be performed on the 10-bit (*pqr stu v wx y*) to get 12-bit (*abcd efgh ijkl*). The indicator bits used for the expansion are vwxst. Indicator bit (v) plays a vital role in the encoding operation—the asterisk mark (*) denotes don't care condition.

Table VIII
The Expansion of 10-bit DPD into 3-Digit Decimal (12-bits)

v	w	x	s	t	a	b	c	d	e	F	g	h	i	j	k	m
0	*	*	*	*	0	p	q	r	0	s	t	u	0	w	x	y
1	0	0	*	*	0	p	q	r	0	s	t	u	1	0	0	y
1	0	1	*	*	0	p	q	r	1	0	0	u	0	s	t	y
1	1	0	*	*	1	0	0	r	0	s	t	U	0	p	q	y
1	1	1	0	0	1	0	0	r	1	0	0	U	0	p	q	y
1	1	1	0	1	1	0	0	r	0	p	q	U	1	0	0	y
1	1	1	1	0	0	p	q	r	1	0	0	U	1	0	0	y
1	1	1	1	1	1	0	0	r	1	0	0	U	1	0	0	y

c. *Boolean logic used for DPD encoding and decoding*

The logic used for the DPD encoding and decoding can be implemented in hardware using Boolean expressions. The expressions provided in Table IX and X which, have been derived from Table VII and VIII, respectively.

Table IX
Boolean Expressions for 12-Bit to 10-Bit in DPD

DPD Bits	Boolean Expressions for Compression into 10 Bits
p	$b\bar{a} + ja\bar{t} + fa\bar{e}i$
q	$c\bar{a} + ka\bar{t} + ga\bar{e}i$
r	*d*
s	$f\bar{e}(\bar{a}\bar{t}) + j(\bar{a}e\bar{t}) + ei$
t	$g\bar{e}(\bar{a}\bar{t}) + k(\bar{a}e\bar{t}) + ai$
u	*h*
v	*a* + *e* + *i*
w	$a + ei + je\bar{t}$
x	$e + ai + k\bar{a}\bar{t}$
y	*m*

Table X
Boolean Expressions for 10-Bit to 12-Bit in DPD

BCD Bits	Boolean Expressions for Expansion into 12 Bits
a	$(vw)(\bar{x} + \bar{s} + (st))$
b	$p(\bar{v} + \bar{w} + (xs\bar{t}))$
c	$q(\bar{v} + \bar{w} + (xs\bar{t}))$
d	*r*
e	$v(\bar{w}x + (wx(s + \bar{t}))$
f	$(s(\bar{v} + (v\bar{x}))) + pvwx\bar{s}t$
g	$(t(\bar{v} + (v\bar{x})))+qvwx\bar{s}t$
h	*u*
i	$v((\bar{w}\bar{x}) + wx(s + t))$
j	$w\bar{v} + sv\bar{w}x + (pvw(\bar{x} + (\bar{s}\bar{t})))$
k	$x\bar{v} + tv\bar{w}x + (qvw(\bar{x} + (\bar{s}\bar{t})))$
m	*y*

IV. Comparative Analysis of Chen-Ho and DPD Coding Techniques

The gate-level design of Chen-Ho [2] and DPD [1] coding techniques have been implemented in MATLAB to analyze bit positioning. Furthermore, for the circuit design prospect, the coding techniques mentioned above have been implemented in Cadence Spectre to evaluate the circuit parameters like average power and delay, using gpdk45 nm technology.

Fig. 4 shows a comparison between Chen-Ho and DPD encodings. In this analysis, 0 to 999 decimal numbers (in 12-bit) have been encoded into 10-bit Chen-Ho and DPD. The 10-bit encoded binary has been converted to a decimal using eqn. 4. This gives an idea of how these two encodings are different from each other.

$$P = \sum_{(i=0)}^{n} 2^i b_i \tag{4}$$

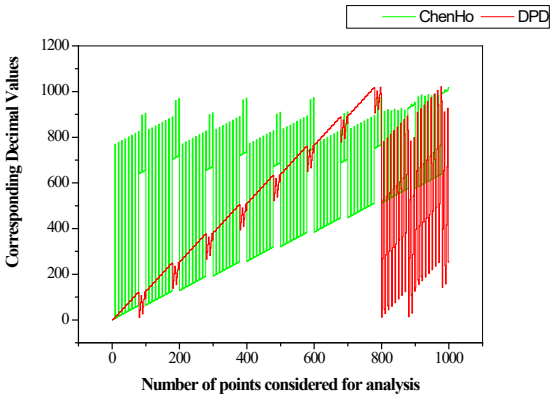

Fig. 4. Representation of DPD and Chen-Ho encoding in decimal

Where $b_0, b_1, b_2 \ldots$ are the binary bits and b_0 is the least significant bit (LSB) starting from the right side, P is the corresponding decimal number.

In Fig. 4, the decimal equivalent of 10-bit Chen-Ho encoding is represented by green color, whereas DPD encoding is marked by red color. The decimal equivalent of both encodings is not providing similar results. The decimal equivalent of 10-bit DPD followed the BCD pattern for ~70%, making DPD a better choice to implement a decimal adder over Chen-Ho.

Meanwhile, in BCD addition, when two numbers are added, and the sum exceeds 9, then 6 is added with the summation result to bring it back into BCD. Meanwhile, in DPD encoding, the encoded decimal numbers followed an excellent pattern in most cases. For example, decimal numbers 0 to 9 are encoded in DPD, and their equivalent binary conversion results in 0000 to 1001. Meanwhile, 10 to 19 are encoded as 10000 to 11001. Similarly, 20 to 29 are encoded as 100000 to 101001 and so on till 79. In this context, it can be observed that the decimal value of the encoded 10-bit DPD shows an increase of 6 for each decade. However, when a larger digit (8 or 9) is present in the 10th or 100th position in the 3-digit decimal number, then the observation mentioned above does not work. It has been observed that the decimal numbers having larger digits in the 10th or 100th place show arbitrary decimal equivalent values of the encoded DPD. When it comes to Chen-Ho encoding, the scenario gets changed completely. Therefore, DPD can be a better choice over Chen-Ho for the implementation of a decimal adder.

In Table V, the equivalent value of the decimal digit 9 for both Chen-Ho and DPD has been shown. Also, from Fig. 1, it is observed that unlike the DPD encoding, which offers more deviation when it represents larger decimal numbers (i.e., more than 778), the Chen-Ho encoding shows more variation when it corresponds to a smaller decimal number (i.e., less than 778). The reason is, Chen-Ho encoding utilizes logic '1' in higher bits (MSBs) for the representation of larger decimal digits (8 and 9), and the decimal conversion of Chen-Ho encoded numbers are much more extensive compared to its actual decimal equivalent. Meanwhile, DPD encoding utilizes lower bits (LSBs) to represent large decimal digits with minimal error. Therefore, DPD based decimal adder will provide a better result than the Chen-Ho-based decimal adder.

Furthermore, the power and delay analysis of the Chen-Ho and DPD encoder and decoder have been performed in Cadence Spectre using gpdk45 nm technology. The results are provided in Table XI.

Table XI
Power and Delay Comparison of Chen-Ho and DPD Encoding and Decoding

Coding Techniques	Encoding Delay	Decoding Delay	Encoding Power	Decoding Power
Chen-Ho	0.1229ns	0.1034ns	1.401mW	3.238mW
DPD	0.0897ns	0.0815ns	1.101mW	2.752mW

Table XI shows that DPD has been dissipating less power and consuming less delay over Chen-Ho encoding and decoding.

These advantages make the DPD encoding a much better option over Chen–Ho encoding for both hardware and software representations of decimal numbers and decimal adder implementation.

V. Implementation of Decimal Adder Using Densely Packed Decimal Coding

BCD adder has some limitations while adding two 3-digit decimal numbers. In order to overcome these limitations, a new methodology has been proposed. This methodology will not only reduce the computational storage requirements but also will speed up the addition process. In addition to the decimal to binary and binary to decimal converter, the proposed DPD-based decimal adder consists of three stages, as shown in Fig. 5.

The decimal to binary converter converts each decimal digit into four binary bits. Therefore, a 3-digit decimal number gets converted into 12-bits binary.

Stage-1: The 12-bits binary (a to m) data is given as input to the DPD encoder, which compresses it to 10-bit data (p to y). In the proposed design, two DPD encoders are used, namely D1 and D2. Both D1 and D2 simultaneously encode 12-bit binary data to 10-bit binary each. These 10-bit outputs are p1 to y1 and p2 to y2 for D1 and D2, respectively.

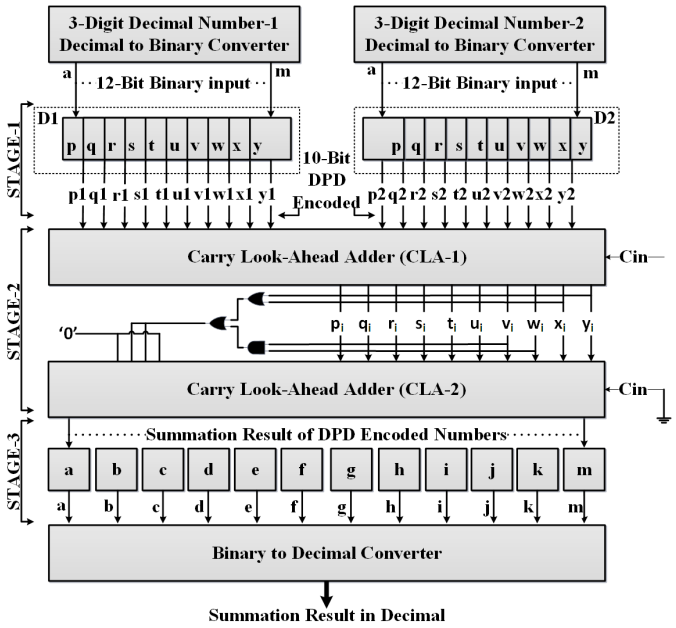

Fig. 5. Proposed DPD based Decimal Adder

Stage-2: In this stage, both the 10-bit DPD encoded numbers, namely p1 to y1 and p2 to y2, are added using CLA-1. Thus summation result (pi to yi) is obtained. This summation result needs correction only when it satisfies the eqn. 5. It can be observed from Table VII that the indicator bits (v_i,w_i,x_i,y_i) give an idea about the larger digit's (8,9) occurrence and value. In CLA-2, The summation result of CLA-1 has been added with the correction value to get the final sum.

$$Corr = (v_i . w_i) + (x_i + y_i) \quad (5)$$

Stage-3: In order to get the final summation result in decimal, the output generated by CLA-2 needs to be converted in the form of a 12-bit binary. Therefore, a DPD decoder circuit is employed. It takes 10-bits as input and provides 12-bit as output (as mentioned in Table X).

VI. Observations and Challenges

The numerical analysis of the existing decimal adder [17] with the proposed one has been shown in Fig. 6. The existing decimal adder's algorithm adds three 4-digit decimal numbers in three stages. In this addition process, initially, adder and analyzer circuit gennnerates Sum *S*[*i*], Carry *C*[*i*], *DGi* and *DPi* signals. Furthermore, the carry network will calculate correction (*Corr*) signal using *DGi* and *DPi* signals. In the last step, all three signals, i.e., Sum *S*[*i*], Carry *C*[*i*], and correction (*Corr*) signals, are added together to get the final sum.

However, in the proposed DPD based decimal adder, a conversion of 12-bits to 10-bits is performed before the addition. Then correction operation has been performed. Subsequently, the final sum is obtained by again converting the 10-bit binary to the 12-bit binary. Hence, the proposed DPD based decimal adder utilizes substantially fewer steps for the addition than the

Existing Decimal Adder [17] Addition Algorithm

Compute:	9234_{10}	X			
	5678_{10}	Y			
+	9876_{10}	Z			
	24778_{10}				

Adder and Analyzer

	Digit-4	Digit-3	Digit-2	Digit-1	
	1001	0010	0011	0100	X
+	0101	0110	0111	1001	Y
+	1001	1000	0111	0110	Z
	0101	1100	0011	1010	S[i]
	10010	00100	01110	01000	C[i]
	0	1	1	1	DG[1]
	1	0	0	0	DG[2]
	0	0	0	0	DP[1]
	0	0	0	0	DP[2]
	0	0	0	0	DP[3]
	1	0	0	1	DP[4]

Carry Network

Cout	Digit-4	Cout	Digit-3	Cout	Digit-2	Cout	Digit-1	
	1		1		1		1	DG[1]
	1		0		0		0	DG[2]
	0		0		0		0	DP[1]
	0		0		0		0	DP[2]
	0		0		0		0	DP[3]
	1		0		0		1	DP[4]
10	1	01	1	01	1	01	1	C_{10}
-	1	-	0	-	0	-	0	C_{20}
0010	1101	0010	0111	0010	0111	0010	0110	Corr

4-Digit Adder

	Cout	Digit-4	Digit-3	Digit-2	Digit-1	
		0101	1100	0011	1010	S[i]
		10010	00100	01110	01000	C[i]
	0010	1101	0111	0111	0110	Corr
	0010	0100	0111	1000	1000	Result

Proposed Decimal Adder Addition Algorithm

	Compute:	554_{10}	X					
	+	118_{10}	Y					
		672_{10}						
	Stage-1:							
Conversion from Binary to DPD	554 in Binary	0101	0101	0100	118 in Binary	0001	0001	1000
	554 in DPD	101	101	0100	118 in DPD	001	001	1000
	Stage-2:							
		101	101	0100	554 in DPD			
	+	001	001	1000	118 in DPD			
		110	110	1100	It needs correction as it is not the right answer			
	Correction = (v.w) + (x+y)				= (1.1)+(0+0)=1			
		110	110	1100	DPD Sum			
	+	000	000	0110	Correction			
		110	111	0010				
Conversion from DPD to Binary	**Stage-3:**							
		110	111	0010	Summation result in DPD			
		0110	0111	0010	Summation result in Binary			
		6	7	2	Summation Result in Decimal			

Fig. 6. Numerical based comparison of existing [17] and proposed decimal adder

reported decimal adder [17], thereby reducing the computational time with less power dissipation.

In this process of adding two decimal numbers, the decimal numbers should be converted to binary for carrying out the addition operation. After the completion of the addition process, the results in binary should be converted back to decimal. Along with all the existing decimal adders [13]-[14], [16]-[17] financial and internet based applications. In this paper a new architecture for efficient Binary coded decimal (BCD, the proposed DPD based decimal adder follow the same procedure. Therefore, the hardware architecture used in the proposed decimal adder is similar to the existing decimal adders. Furthermore, the simulation result for the decimal to binary conversion and binary to decimal conversion has been calculated in Cadence Spectre and provided in Table XII.

Table XII
Power and Delay Comparison of Decimal to Binary and Binary to Decimal Conversion Modules

Parameters	Decimal to Binary	Binary to Decimal
Power (mW)	0.878	0.667
Delay (ns)	0.0313	0.0222

Circuit level implementation of the proposed DPD based decimal adder and the reported adders [13]-[14]financial and internet based applications. In this paper a new architecture for efficient Binary coded decimal (BCD has been implemented in Cadence Spectre. The performance parameters like power and delay have been extracted in Cadence Spectre using gpdk45 nm technology. All the possible outputs for the decimal numbers' input combinations between 0 to 999 have been observed.

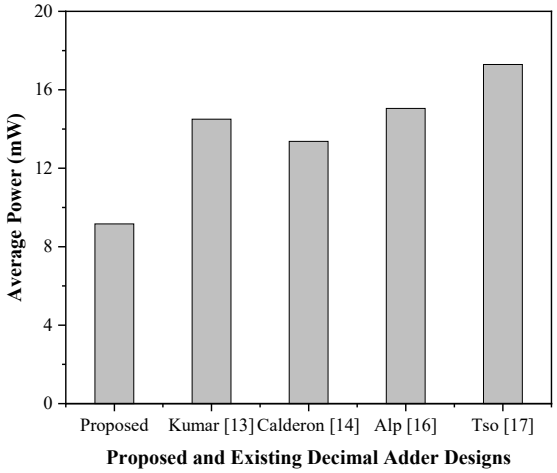

Fig. 7. Average Power of the Proposed and Existing Decimal Adders

Analysis of average power consumption is shown in Fig. 7. The existing decimal adder design [17] is consuming more power, followed by [16]-[13]-[14]. In contrast, the proposed decimal adder is consuming less power as compared withall existing reported architectures.

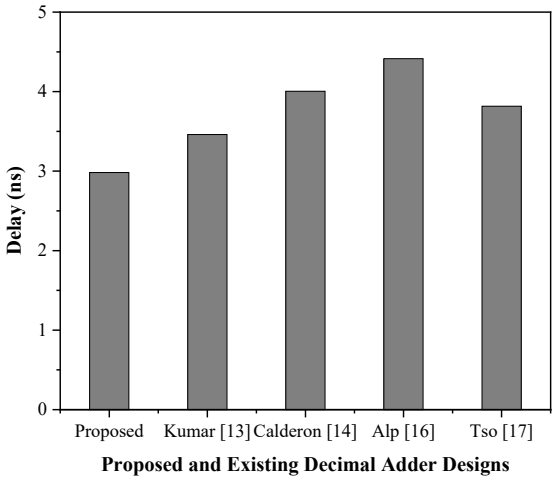

Fig. 8. Delay of the Proposed and Existing Decimal Adders

In Fig. 8, it has been observed that the proposed decimal adder produces the least delay in comparison to the existing adders [13]-[14], [16]-[17].

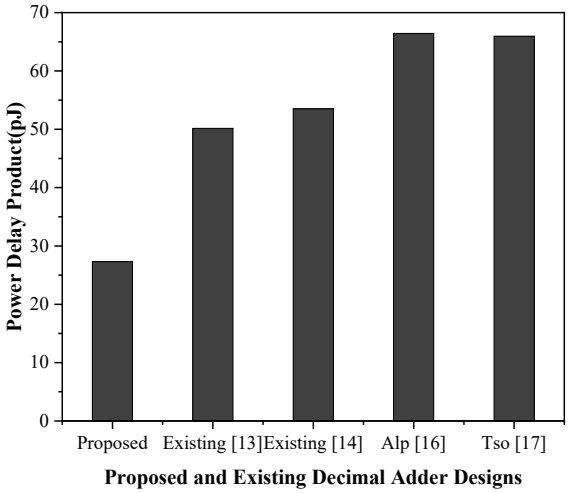

Fig. 9. PDP of the Proposed and Existing Decimal Adders

Fig. 9 shows the power delay product analysis of the existing and the proposed decimal adders. It is concluded that the proposed decimal adder offers substantially improved performance parameters than its counter-parts [13]-[14], [16]-[17].

Comparison of BCD and Binary based Decimal Adder

Addition of two decimal numbers using binary adders, both the decimal digits have to convert into binary. Therefore, the double-dable method (division by 2) is used [17], where each decimal digit is successively divided by 2. The remainders generated in each step are considered together as the corresponding binary equivalent. However, in BCD, each decimal digit is represented by 4-bits using 8421 encodings. For example, consider a decimal digit 997 whose BCD representation is 1001 1001 0111, whereas its binary representation is 1111100101. In

this conversion, since the encoding is carried out in parallel, only one encoder delay have to consider. However, due to the successive division of the decimal number by 2, the size of the encoder circuit and delay increases significantly in decimal to binary conversion. Moreover, the encoder size and propagation delay are proportionally increasing with the size of decimal number. On the other hand, the addition operation is performed using carry propagate adder (CLA/RCA) in both the binary-based decimal adder and BCD-based decimal adders. However, the BCD-based decimal adder requires extra circuitry for correction.

The corresponding summation result is in binary, and this needs to get converted back to decimal. With the help of eqn. 4, binary to decimal conversion is performed. Meanwhile, the BCD-based summation result is grouped into 4-bits starting from LSB and decoded back to decimal. The delay of the binary to decimal conversion depends on the length of the summation result generated, whereas in BCD, it depends upon only one BCD to decimal decoder delay. Although the addition process using binary adders depends upon carry propagate adder only, conversion of decimal to binary and binary to decimal increases the overall delay. In this process of decimal addition using binary adders, the main disadvantage is the conversion of decimal to binary and binary to decimal.

Therefore, to justify, binary adder-based decimal adder has been implemented in Cadence Spectre and the average power and minimum delay has been extracted using gpdk 45nm technology. It's noteworthy that circuits are evaluated at three different stages, and results are provided in Table XIII.

Table XIII
Power and Delay Comparison of Binary and BCD Based Decimal Adders

Decimal Adder	Parameters	Decimal to Binary	CLA/RCA Addition	Binary to Decimal
Using Binary Adders	Power(mW)	2.212	6.02	0.894
	Delay(ns)	1.823	0.76	1.132
Using BCD Adders	Power(mW)	0.878	9.67	0.667
	Delay(ns)	0.0313	2.88	0.0222

It is observed from Table XIII that the decimal adder based on binary adder shows 22.8% of improvement in overall power dissipation over its counter-part. However, the BCD adder-based decimal adder gains 26.6% in delay over the binary adder-based decimal adder.

Furthermore,the conversion of floating-point decimal numbers into binary causes recurring infinity bits. Thereby, the converted decimal fraction number becomes incorrect and causes approximate errors [17]. However, DPD based encoding can convert floating-point decimal numbers in binary registers efficiently without any loss [1]. Therefore, BCD adder-based decimal adders are preferred as a better choice while making decimal adder over binary adder-based decimal adder.

A. Challenges associated with Decimal adder using DPD Coding Technique

The addition of two decimal numbers using DPD encoding has not given correct results for all possible additions. The addition of two three-digit decimal numbers is offering 84.44% correct outputs. The reason is, while adding two DPD numbers through RCA/CLA, the summation result becomes 11-bits due to the generation of a carry. The expansion algorithm of DPD can convert 10-bit DPD to 12-bit, whereas the summation output is 11-bits. Therefore, it is not possible to convert 11-bit DPD to binary.

B. Possible Solutions

The addition result can be error-free by taking some of the necessary steps:

1. Instead of adding three-digit decimal numbers, we can add two-digit decimal numbers by replacing the left-most digit with '0' padding. This will give the correct result of 94.06%.
2. Apart from the DPD module, an error recovery circuit can reduce the error to zero.

VII. Application: Image Addition

An arithmetic circuit plays a vital role in image processing. Decimal adders' performance evaluation can be validated through image processing applications like image addition, image compression, etc. Therefore, to analyze the results' betterment, researchers have implemented various image processing applications in their research [18]–[20]. Researchers in [18] have performed an image denoising operation on a 128×128 Lena image. They have used a weighted average filter for the removal of salt and pepper noise. Their proposed adders have replaced the adders used in the weighted average filters.

Similarly, the researchers in [19]-[20] have performed image compression and decompression with the help of discrete cosine transform (DCT) and inverse discrete cosine transform (IDCT). In the DCT and IDCT module's hardware realization, all arithmetic adders have been replaced by their proposed adders for the analysis. Therefore, to analyze the proposed adder's exactness, the existing decimal adders [13]-[14] have been considered for comparison.

a. Image Addition

For the validation of the proposed decimal adder's performance, the image addition application has been performed.For image addition, two identical-sized images are taken as input and produce a third image of the same size. The addition of two images is performed straightforwardly on a pixel-by-pixel basis, as shown in eqn. 6.

$$P(x,y) = Q_1(x,y) + Q_2(x,y) \tag{6}$$

In this task, two 128×128 sized images named apple.jpg and rose.jpg have been considered for addition. The addition operation has been performed by the proposed DPD-based decimal adder based upon pixel by pixel addition. Each pixel contains a

particular value within the range of 0 to 255. The corresponding decimal value of each pixel of both images needs to convert into 10-bit DPD. Then the addition operation has been performed using CLA, followed by the correction stage. The related addition result is again converted back to decimal. The resulting image has shown in Fig. 10.

Fig. 10. Image addition results

In this context, an image addition application has been utilized to show the proposed adder's effectiveness. In this addition process, existing decimal adders [13]-[14] add corresponding pixels of two identical sized images. Each pixel contains a particular decimal value and is expressed in 12-bits. Meanwhile, the proposed DPD-based decimal adder requires only 10-bit addition, saving computational storage space and improving the overall addition process's delay.

b. Structural Similarity Index Metric (SSIM)

Structural Similarity Index Metric has been used to determine the structural similarity between two images. The resultant image might have some irregularities, whereas the reference image should be distortionless. SSIM is a perception-based approach and less complex in nature. Thus SSIM is preferred over Mean Square Error (MSE) and Peak Signal to Noise Ration (PSNR). The SSIM value always lies between -1 to 1. The degree of exactness is more when the SSIM value approaches towards 1, and the difference is more when it approaches -1. The SSIM values arecalculated from the proposed, and existing adders [13]-[14] have been shown in Fig. 11 and Fig. 12.

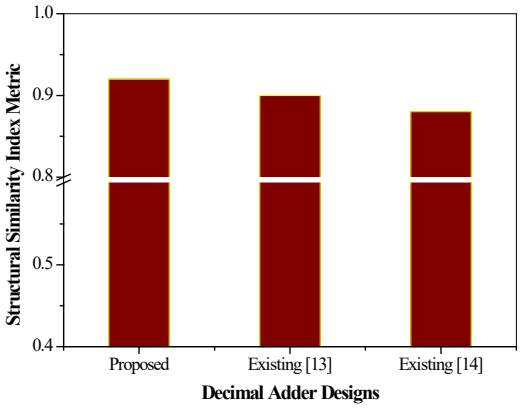

Fig. 11. SSIM values for the proposed and existing decimal adders

Fig. 12. (a) Proposed, (b) Existing [13], (c) Existing [14] Structural similarity pictorial representation

The SSIM results depicted in Fig. 11 and Fig. 12 show that all three decimal adders provide nearly the same addition result. However, the proposed adder's results are better than its counter-part [13]-[14].

V. Conclusions

In this manuscript, comparative analysis as a function of VLSI parameters like delay and power of Chen-Ho and DPD coding techniques has been addressed. Unlike Chen-Ho, the bit-positioning in DPD coding is right-aligned, which reduced the overall error when implemented in a decimal adder. In addition to it, the DPD based decimal adder dissipated less power and delay compared to the reported decimal adders. The proposed DPD based decimal adder has ~84.44% correct output for the addition of two three-digit decimal numbers, for which several error-free solutions are also addressed. It would be a welcome approach for the researchers to design the error recovery module and reduce the architecture of the DPD based decimal adder.

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Harmonic Elimination in Uniform Step Nine-Level Inverter Using Differential Evolution: Experimental Validation

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***Abstract*—This study presents the application of differential evolution algorithm to compute optimal switching angles for a single-phase nine-level inverter to improve the output voltage quality. The topology of the proposed inverter in this article is a simple cascade converter composed of two H-bridge cells with non-equal DC voltage sources in order to generate multiple voltage levels. Selective harmonic elimination pulse width modulation strategy is used to improve the generated AC output voltage waveform. The differential evolution optimization algorithm is used to solve non-linear transcendental equations necessary for the (SHPWM). Computational results obtained from computer simulations presented a good agreement with the theoretical predictions. A laboratory prototype based on STM32F407 microcontroller was built in order to validate the simulation results. The experimental results show the effectiveness of the proposed modulation method.**

***Index Terms*—Multi-level inverters; selective harmonic elimination; differential evolution; optimization; STM32F407 microcontroller.**

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I. Introduction

The cascade multilevel power inverters have received a lot of attention because of their simple and modular structure; these converters can offer a lot of advantages such as low switching losses [1]-[3] and better electromagnetic compatibility [4]-[5], low voltage stress on the switching devices [6]. The architecture can be formed by simply connecting multiple H-bridge cells in series, by adding more cells, the output voltage waveform become close to a sinusoidal waveform. Several modulation strategies such as Sinusoidal Pulse width modulation (SPWM) [7] and space vector pulse width modulation (SVPWM) [8] have been proposed for the control of multilevel inverters. A more efficient method called selective harmonic elimination pulse width modulation (SHEPWM) is also used; the method offers a lot of advantages such as operating the inverters switching devices at a low frequency which extends the lifetime of the switching devices. The main disadvantage of this method is that a set of non-linear equations must be solved to obtain the optimal switching angles to apply this strategy.

Multiple computational methods have been used to solve the optimal switching problem for multilevel inverters, and Newton-Raphson (N-R) algorithm [9] is one of the most used methods for solving SHEPWM equations, this method dependents on initial guess of the angle values in such a way that they are sufficiently close to the global minimum(desired solution). If the angles are unsuitable, non-convergence can result. Another method to compute the optimal switching angles is by using optimization algorithms such as genetic algorithm (GA) [10]-[11], particle swarm operation (PSO) [12]-[14] and bee algorithm (BA) [15]. The main advantage of these methods is that they are free from the requirement of good initial guess.

Differential evolution (DE) is one of the most powerful optimization methods. The algorithm has been drawing a lot of attention since its introduction in 1997. The DE is a simple yet powerful algorithm; it is composed of three main operations mutation, crossover and selection. The algorithm uses the difference of solution vectors to create new candidate solutions using the above-mentioned operators. This work investigates the use of (DE) as an optimization tool to implement the (SHEPWM) for a nine level inverter.

This article presents a simple and fast optimal solution of harmonic elimination of a nine level inverter with non-equal DC sources using the DE algorithm. The algorithm is used to solve a set of non-linear equations in order to obtain the optimal switching angles with the goal of eliminating low order harmonics (3^{rd}, 5^{th}, 7^{th}).

This paper is organized as follows: the next section explains briefly the structure of the proposed multilevel inverter and its control, the third section covers the application of the differential evolution algorithm for the selective harmonic elimination, this section details the procedures to obtain the optimal switch-

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ing angles and the formulation of the objective function, the fourth section presents the simulation results obtained from the mathematical model of the system and the optimization method. The effectiveness of the selective harmonic elimination using DE is verified using a small scale laboratory nine-level inverter based on STM32F407 Microcontroller unit. The conclusion is presented in the last section.

II. Topology

The cascaded multilevel inverter topology depends on one simple principle which is based on the addition of the voltage that is generated by each individual cell (H-bridge) in order to obtain a staircase output voltage waveform.

Table 1. Switching logic of a nine level H-bridge inverter

	Switches state							
Voltage levels (*p.u*)	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
4	on	off	off	on	on	off	off	on
3	off	on	off	on	on	off	off	on
2	off	on	on	off	on	off	off	on
1	on	off	off	on	off	on	off	on
0	off	on	off	on	off	on	off	on
-1	off	on	on	off	off	on	off	on
-2	on	off	off	on	off	on	on	off
-3	off	on	off	on	off	on	on	off
-4	off	on	on	off	off	on	on	off

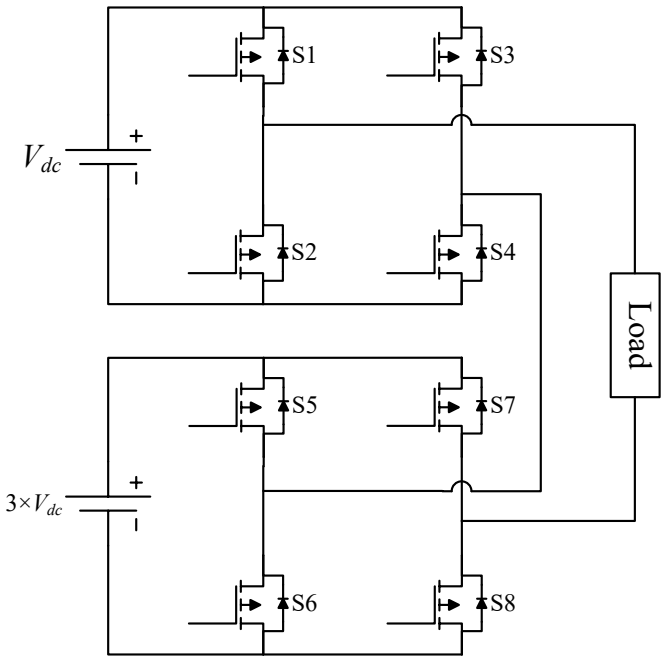

Fig. 1. Schematic of the proposed converter

Fig. 1 reveals the proposed single-phase asymmetrical nine-level inverter. It is shaped by two H-bridges that are connected indifferent series with each bridge can be powered by power supplies that are electrically isolated in order to generate the wanted waveform.

Every module can generate three voltage levels +V which is the positive voltage of the DC source, 0V and –V which represents the DC source negative voltage, and as it is demonstrated in Fig.1 when wanting to obtain nine voltage levels from the proposed inverter, the DC voltage source that is connected to the lower cell must be three times its value of the DC source that is this time connected to the upper cell ($V_{dc2}=3\times V_{dc1}$). Table 1. Shows the switching states of all the possible combinations for the asymmetrical nine-level inverter.

III. Selective Harmonic Elimination Using Differential Evolution

The number of voltage levels that can be generated by CMLIs is generally presented by *2P + 1* where P represents the number of voltage levels or switching angles in a quarter waveform of the signal with P-1 is representing the number of undesired harmonics that can be removed from the generated waveform.

When using a nine-level inverter, four is the number of voltage levels in the quarter waveform. This means that the number of harmonics that can be eliminated is three. Fig. 2 shows the voltage waveform in a quarter of period for a nine-level inverter where the switching angles θ_1, θ_2, θ_3, and θ_4 must be computed in a designed way allowing the control of the fundamental component and the elimination of undesired harmonics.

There are four voltage levels (in the quarter waveform) and three undesired harmonics for the staircase output voltage waveform of the multilevel inverter as illustrated in Fig. 2.

In order to control the peak value of the output voltage to be V_1 along with eliminating the 3rd, 5th, and 7th harmonic and considering the voltage waveform has quarter and half-wave symmetry characteristics thus the resulting Fourier series expansion is given as:

$$V(\omega t)=\sum_{n=1,3,5,\ldots}^{\infty}\left[\frac{4V_{dc}}{n\pi}\sum_{i=1}^{p}\cos(n\theta_i)\right]\sin(n\omega t) \tag{1}$$

Where *n* is rank of harmonics, $n = 1, 3, 5, \ldots$, and $p = (N - 1)/2$ is the number of switching angles per quarter waveform., and θ_i is the i^{th} switching angle, and N is the number of voltage levels per half waveform.

$$\begin{cases} H_1=\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)=((\dfrac{N-1}{2})\times\dfrac{r}{4}) \\ H_3=\cos(3\theta_1)+\cos(3\theta_2)+\cos(3\theta_3)+\cos(3\theta_4)=0 \\ H_5=\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)=0 \\ H_7=\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)=0 \end{cases} \tag{2}$$

Where r is the modulation index.

We put $M = ((\frac{N-1}{2})(\frac{r}{4}))$.

The obtained solutions must satisfy the following constraint:

$$0 \prec \theta_1 \prec ... \prec \theta_P \prec \frac{\pi}{2} \tag{3}$$

When performing the optimization process it is fundamental to use an objective function. This function must be formulated in a way that allows the elimination of the chosen harmonics and also allows maintaining the amplitude of the fundamental component at the desired value consequently the objective function is defined as:

$$F(\theta_1\theta_2...\theta_p) = (\sum_{n=1}^{p}\cos(\theta_n) - M)^2 + (\sum_{n=1}^{p}\cos(3\theta_n))^2 + (\sum_{n=1}^{p}\cos(5\theta_n))^2 + (\sum_{n=1}^{p}\cos(7\theta_n))^2 \tag{4}$$

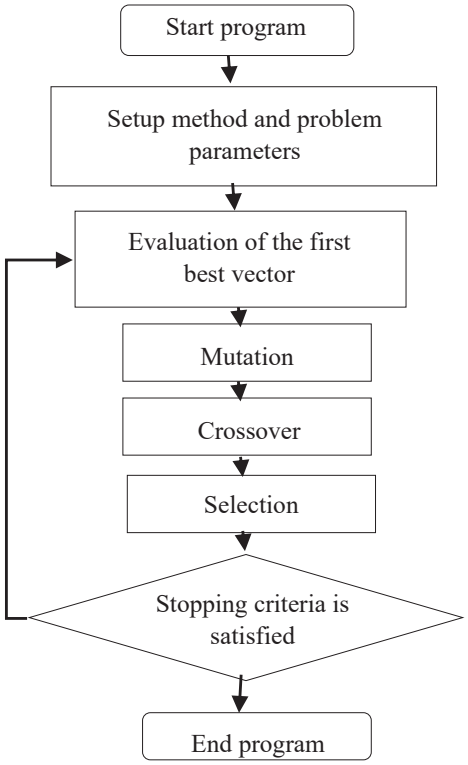

Fig. 3. Flowchart of DE algorithm

The optimal switching angles can be obtained by minimizing (4) subject to the constraint (3). The differential algorithm is used to overcome the main problem which is the non-linearity of the transcendental set of (2). The three main steps that include initialization, mutation and crossover are composing the algorithm. Fig. 3 illustrates the general structure of a DE program. When employing the mutation, the algorithm perturbs the population of vectors through its diversity is controlled by the cross-over process [16].

For the SHPWM strategy, the DE algorithm is used as an optimization tool to perform a random search for the global minima, which is forcing the objective function (4) towards an acceptable error value.

The optimization process begins by initializing the indispensable algorithm parameters like the crossover probability (CP), upper and lower bounds (θ_{min} and θ_{max}), population size (NP) and the maximum number of iterations. It is worth noting that the boundaries have to satisfy equation (3). The further stage is to arbitrary generating an initial population of switching angles in this process the algorithm produces.

$$\theta_{ij}^{(0)} = \theta_{\min ij} + rand_i(\theta_{mawj} - \theta_{\min j}) \tag{5}$$

with i = 1, 2,…,NP and j = 1, 2 ,…, N

Where $\theta_{ij}^{(0)}$ represents the initial population, i mean the population size in this study NP=75, j represents the number of decision variables that constitute the number of switching angles, in case of a nine-level inverter N=4. Following the initialization process, the evaluation of the generated population is done. Furthermore, the fitness of each individual evaluation is carried out by using (4).

Based on the initial population, a mutant v_{ij} vector is created by the mutation process. This process is outlined by the following expression:

$$v_{ij} = X_{r1} + F(X_{r2} - X_{r3}) \tag{6}$$

X_r1, X_{r2} and X_{r3} are vectors randomly sampled from the generated population, $X_r = [\theta_{i1}, \theta_{i2}, ..., \theta_{iN}]$, the indices *r1, r2* and *r3* are integers randomly chosen from the range [1 NP] and are as well chosen to be different from the index i, the F parameter is the mutation constant which controls the amplification of the differential variation $(X_{r2} - X_{r3})$, this parameter value is randomly generated from the range [0 1], it should be pointed out that multiple mutation methods were reported in [17].

The crossover operation comes into play in order to improve the diversity of the population after generating the mutant vector v_{ij} through mutation. This operation satisfies the production of fitter individuals with the result is a vector u that is obtained by mixing the components of v_{ij} and X_i. The process can be expressed as:

$$u = \begin{cases} v_{ij} \; if \quad rand \le CP \quad or \quad j = j_{rand} \\ X_i \quad otherwise \end{cases} \tag{7}$$

Where rand represents a random number in the range of [0 1], CP represents the crossover probability constant which controls the diversity of the population and a value between 0 and 1 [18], j_{rand} is an index that is randomly chosen. Once the crossover process is completed, the selection process comes into play to decide whether the u_i or X_i vector survives for the next generation, this process is carried out to choose the fittest individual. The selection process can be expressed mathematically as:

$$X_i^{G+1} = \begin{cases} u_i^{G+1} \quad if \quad f(u_i^{G+1}) \prec \quad f(X_i^G) \\ X_i^G \quad otherwise \end{cases} \tag{8}$$

where $f(X)$ represents the objective function to be minimized and G represents the generation count. After the selection operation is completed, the algorithm loop is repeated up to the stopping criteria is satisfied, in this work the DE algorithm is restricted by maximum number of iterations N_{itr} = 1000.

IV. Simulation Result

In order to demonstrate the theoretical predictions as well as to test the effectiveness of the proposed algorithm, the proposed inverter and the control method were developed then simulated using MATLAB/SIMULINK for scientific programming environment. A computer with Intel(R) Core(TM) i3 CPU@ 2.13GHz Processor and 4GB of RAM was used in order to execute the optimization program. It takes for the optimization algorithm 1549.37 seconds to complete the computation process.

For verifying the proposed method's effectiveness the Total Harmonic Distortion (THD) was used as a performance indicator in order to evaluate the quality of output AC voltage waveform generated from the multi-level inverter. Moreover, the THD is defined as the total amount of harmonics related to the fundamental which can be calculated using the subsequent formula:

$$THD = \frac{\sqrt{\sum_{n=3}^{19} H_n^2}}{H_1} \times 100 \tag{9}$$

The DE algorithm is used to observe the switching angles for every value of modulation index r; also, for each r the total harmonic distortion is also computed.

The optimal switching angles (in degrees) versus modulation index r with $r \in [0.2\ 1.1]$ are shown in Fig. 4 while the angles are computed with a fine step-size of 0.01.

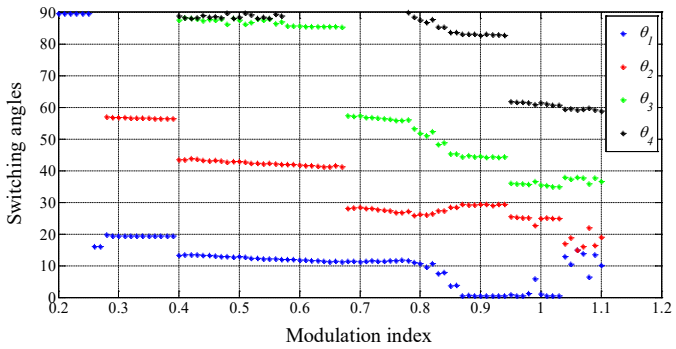

Fig. 4. Optimal switching angles obtain by DE algorithm versus modulation index

It can be seen that in some ranges of the modulation index such as $r \in [0.2\ 0.4]$ and also $\in [0.6\ 0.72]$, the obtained solutions exceeded the 90 degrees limit, these switching angles should not be taken into account. Fig. 5 shows the variation of the total harmonic distortion versus the modulation index, these results are obtained by using (8) and (2).

The validity of the proposed algorithm is to be confirmed. From the obtained switching angles we extracted angles that were applied to the mathematical model of the nine-level inverter. The output voltage obtained from the multilevel inverter for r=0.85 is illustrated in Fig. 6.

Fig. 7 shows the FFT analysis of the output voltage waveform. It can be clearly seen from the FFT analysis that the selected harmonics (3rd, 5th and 7th) are successfully eliminated, the total harmonic distortion of the generated waveform was found to be THD=14.12%.

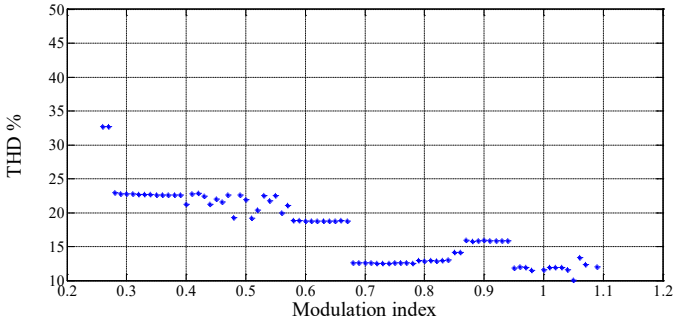

Fig. 5. Total harmonic distortion versus modulation index

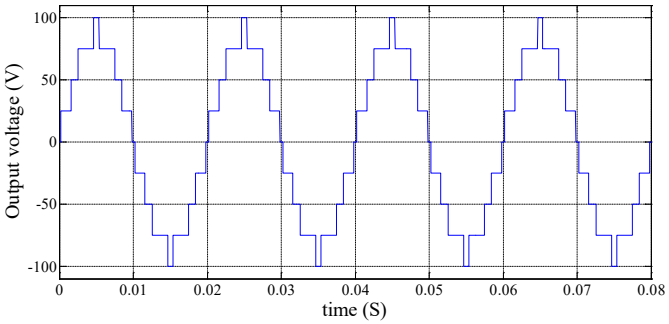

Fig. 6. Simulation results of output voltage waveform

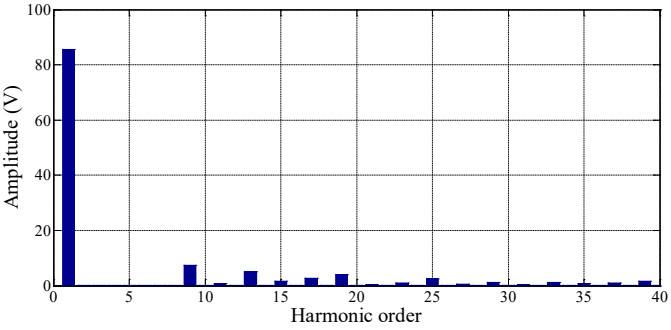

Fig. 7. FFT analysis for r =0.85

V. Experimental Results

The proposed method was validated by building a small scale laboratory prototype used as switching devices IRF640(200V,18A) MOSFETs, SDS1000 oscilloscope 100MHz 500Ms/s which was used to capture the voltage waveforms. In addition, in order to generate control signals for the switching devices a STMF407 microcontroller was used. A computer connected to the oscilloscope through USB was used for the FFT analysis. The experimental validation of the single phase nine-level voltage pattern obtained in simulation is shown in Fig. 6 and 7 illustrates and the results are illustrated in Fig. 9.

Fig. 9 illustrates the FFT analysis of the experimentally obtained voltage waveform; it can be clearly seen that the 3rd, 5th and the 7th harmonic were successfully eliminated. This result matches completely the simulation result seen in Fig. 7

The total harmonic distortion of the experimental voltage waveform is 14.20% which is very close to the simulation result. Fig. 10 and Fig. 11 demonstrates the experimental gating signals for the semiconductor switches from S1 to S8.

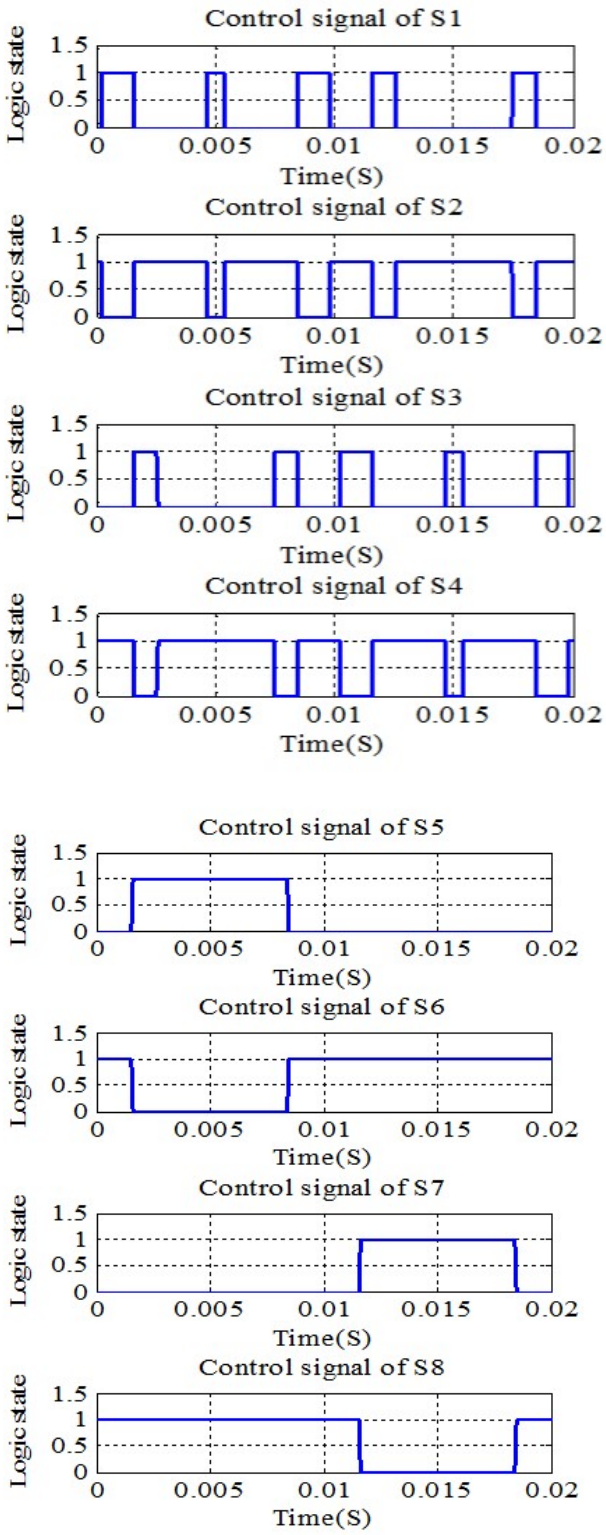

Fig. 8. Simulation results of gating signals

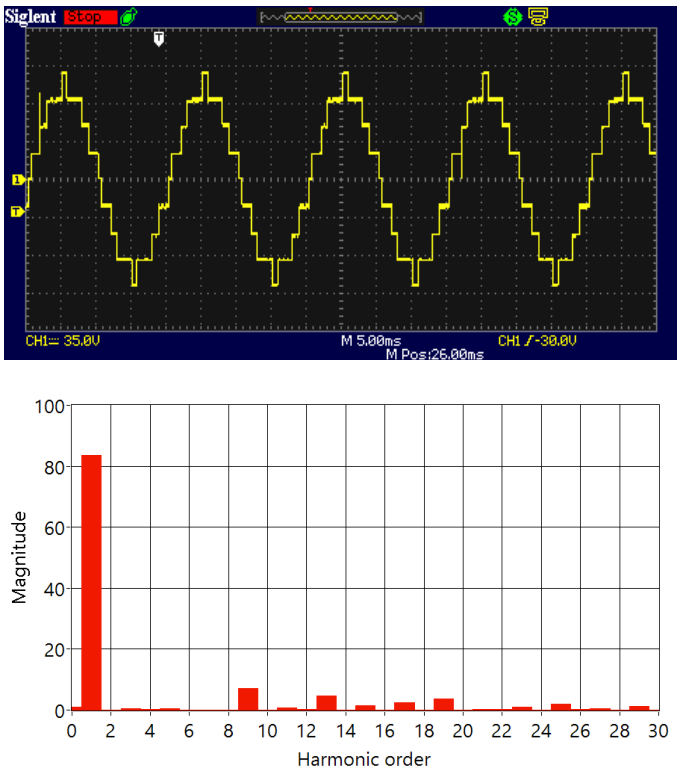

Fig. 9. Experimental result of the output voltage and the corresponding FFT analysis

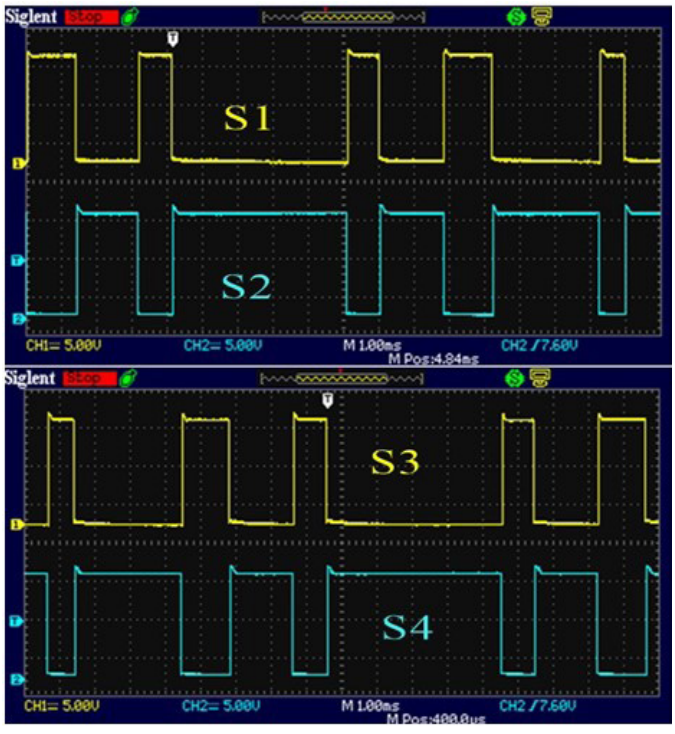

Fig. 10. Experimental gating signal waveforms for the semiconductor switches from S1 to S4.

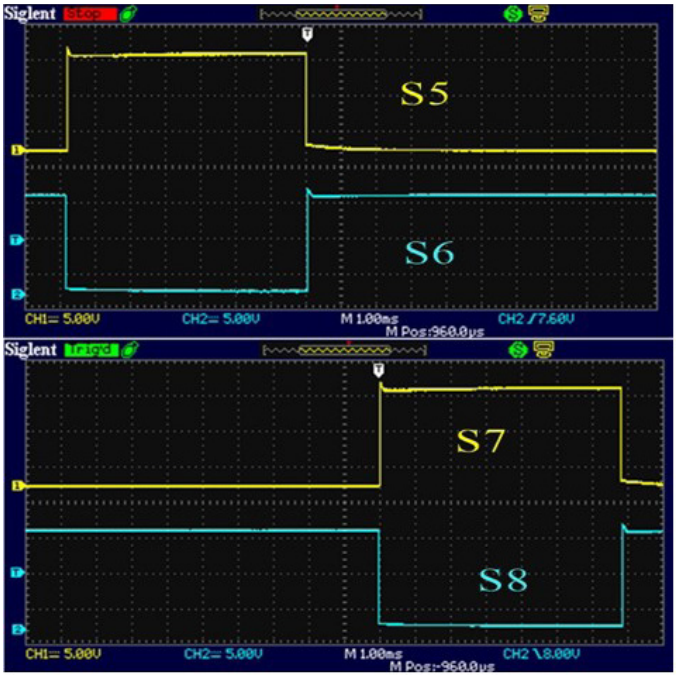

Fig. 11. Experimental gating signal waveforms for the semiconductor switches from S5 to S8.

VI. Conclusion

This study demonstrates the application of the DE algorithm in selective harmonic elimination for a nine-level voltage source cascade inverter which can improve the harmonic quality of the generated output voltage. The proposed inverter topology with non-equal DC sources has the advantage of generating nine voltage levels with less switching components.

The DE algorithm is used to solve a set of non-linear equations in order to obtain the optimal switching angles to perform the (SHE) modulation strategy.

The validity of the method has been confirmed by computer simulation using Matlab/Simulink scientific programming environment and verified by experimental hardware set-up based on STM32F407 microcontroller. The results from the hardware and simulation show a good agreement with the theoretical prediction.

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Preparation of Papers for Electronics (September 2011)

First A. Author, Second B. Author, and Third C. Author

***Abstract*—These instructions give you guidelines for preparing papers for ELECTRONICS journal. Use this document as a template if you are using Microsoft *Word* 6.0 or later. Otherwise, use this document as an instruction set. The electronic file of your paper will be formatted further. Define all symbols used in the abstract. Do not cite references in the abstract. Do not delete the blank line immediately above the abstract; it sets the footnote at the bottom of this column.**

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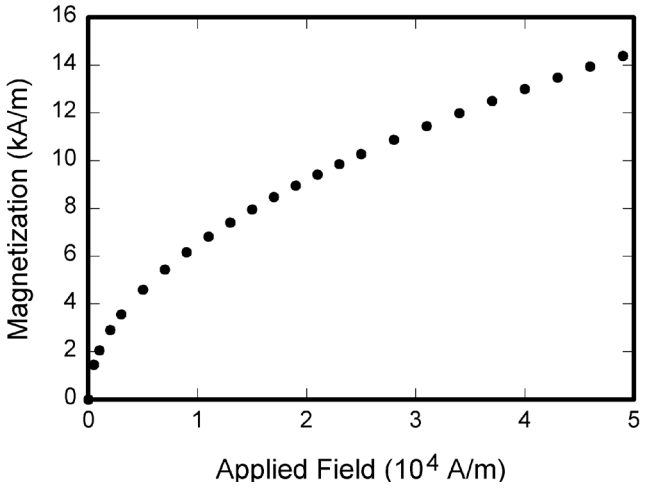

Fig. 1. Magnetization as a function of applied field. Note that "Fig." is abbreviated. There is a period after the figure number, followed by two spaces. It is good practice to explain the significance of the figure in the caption.

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Use either SI (MKS) or CGS as primary units. (SI units are strongly encouraged.) English units may be used as secondary units (in parentheses). **This applies to papers in data storage.** For example, write "15 Gb/cm^2 (100 Gb/in^2)." An exception is when English units are used as identifiers in trade, such as "3½-in disk drive." Avoid combining SI and CGS units, such as current in amperes and magnetic field in oersteds. This often leads to confusion because equations do not balance dimensionally. If you must use mixed units, clearly state the units for each quantity in an equation.

The SI unit for magnetic field strength H is A/m. However, if you wish to use units of T, either refer to magnetic flux density B or magnetic field strength symbolized as $\mu_0 H$. Use the center dot to separate compound units, e.g., "A·m^2."

TABLE I
Units for Magnetic Properties

Symbol	Quantity	Conversion from Gaussian and CGS EMU to SI [a]
Φ	magnetic flux	1 Mx $\rightarrow 10^{-8}$ Wb = 10^{-8} V·s
B	magnetic flux density, magnetic induction	1 G $\rightarrow 10^{-4}$ T = 10^{-4} Wb/m^2
H	magnetic field strength	1 Oe $\rightarrow 10^3/(4\pi)$ A/m
m	magnetic moment	1 erg/G = 1 emu $\rightarrow 10^{-3}$ A·m^2 = 10^{-3} J/T
M	magnetization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 10^3$ A/m
$4\pi M$	magnetization	1 G $\rightarrow 10^3/(4\pi)$ A/m
σ	specific magnetization	1 erg/(G·g) = 1 emu/g $\rightarrow$ 1 A·m^2/kg
j	magnetic dipole moment	1 erg/G = 1 emu $\rightarrow 4\pi \times 10^{-10}$ Wb·m
J	magnetic polarization	1 erg/(G·cm^3) = 1 emu/cm^3 $\rightarrow 4\pi \times 10^{-4}$ T
χ, κ	susceptibility	1 $\rightarrow 4\pi$
χ_ρ	mass susceptibility	1 cm^3/g $\rightarrow 4\pi \times 10^{-3}$ m^3/kg
μ	permeability	1 $\rightarrow 4\pi \times 10^{-7}$ H/m = $4\pi \times 10^{-7}$ Wb/(A·m)
μ_r	relative permeability	$\mu \rightarrow \mu_r$
w, W	energy density	1 erg/cm^3 $\rightarrow 10^{-1}$ J/m^3
N, D	demagnetizing factor	1 $\rightarrow 1/(4\pi)$

Vertical lines are optional in tables. Statements that serve as captions for the entire table do not need footnote letters.

[a]Gaussian units are the same as cgs emu for magnetostatics; Mx = maxwell, G = gauss, Oe = oersted; Wb = weber, V = volt, s = second, T = tesla, m = meter, A = ampere, J = joule, kg = kilogram, H = henry.

V. Helpful Hints

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Because we will do the final formatting of your paper, you do not need to position figures and tables at the top and bottom of each column. In fact, all figures, figure captions, and tables can be at the end of the paper. Large figures and tables may span both columns. Place figure captions below the figures; place table titles above the tables. If your figure has two parts, include the labels "(a)" and "(b)" as part of the artwork. Please verify that the figures and tables you mention in the text actually exist. **Please do not include captions as part of the figures. Do not put captions in "text boxes" linked to the figures. Do not put borders around the outside of your figures.** Use the abbreviation "Fig." even at the beginning of a sentence. Do not abbreviate "Table." Tables are numbered with Roman numerals.

Color printing of figures is not available Do not use color unless it is necessary for the proper interpretation of your figures.

Figure axis labels are often a source of confusion. Use words rather than symbols. As an example, write the quantity "Magnetization," or "Magnetization *M*," not just "*M*." Put units in parentheses. Do not label axes only with units. As in Fig. 1, for example, write "Magnetization (A/m)" or "Magnetization ($A \cdot m^{-1}$)," not just "A/m." Do not label axes with a ratio of quantities and units. For example, write "Temperature (K)," not "Temperature/K."

Multipliers can be especially confusing. Write "Magnetization (kA/m)" or "Magnetization (10^3 A/m)." Do not write "Magnetization (A/m) x 1000" because the reader would not know whether the top axis label in Fig. 1 meant 16000 A/m or 0.016 A/m. Figure labels should be legible, approximately 8 to 12 point type.

B. References

Number citations consecutively in square brackets [1]. The sentence punctuation follows the brackets [2]. Multiple references [2], [3] are each numbered with separate brackets [1]–[3]. When citing a section in a book, please give the relevant page numbers [2]. In sentences, refer simply to the reference number, as in [3]. Do not use "Ref. [3]" or "reference [3]" except at the beginning of a sentence: "Reference [3] shows ... ." Please do not use automatic endnotes in *Word*, rather, type the reference list at the end of the paper using the "References" style.

Number footnotes separately in superscripts (Insert | Footnote).[1] Place the actual footnote at the bottom of the column in which it is cited; do not put footnotes in the reference list (endnotes). Use letters for table footnotes (see Table I).

Please note that the references at the end of this document are in the preferred referencing style. Give all authors' names; do not use "*et al*." unless there are six authors or more. Use a space after authors' initials. Papers that have not been published should be cited as "unpublished" [4]. Papers that have been accepted for publication, but not yet specified for an issue should be cited as "to be published" [5]. Papers that have been submitted for publication should be cited as "submitted for publication" [6]. Please give affiliations and addresses for private communications [7].

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Define abbreviations and acronyms the first time they are used in the text, even after they have already been defined in the abstract. Abbreviations such as IEEE, SI, ac, and dc do not have to be defined. Abbreviations that incorporate periods should not have spaces: write "C.N.R.S.," not "C. N. R. S." Do not use abbreviations in the title unless they are unavoidable (for example, "IEEE" in the title of this article).

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Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). First use the equation editor to create the equation. Then select the "Equation" markup style. Press the tab key and write the equation number in parentheses. To make your equations more compact, you may use the solidus (/), the exp function, or appropriate exponents. Use parentheses to avoid ambiguities in denominators. Punctuate equations when they are part of a sentence, as in

$$\int_0^{r_2} F(r,\varphi)\,\mathbf{d}\,d\varphi = [\sigma r_2/(2\mu_0)] \cdot \int_0^{\infty} \exp(-\lambda\,|z_j - z_i|)\,\lambda^{-1} J_1(\lambda r_2)\,J_0(\lambda r_i)\,d\lambda\,. \tag{1}$$

Be sure that the symbols in your equation have been defined before the equation appears or immediately following. Italicize symbols (*T* might refer to temperature, but T is the unit tesla). Refer to "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ... ."

E. Other Recommendations

Use one space after periods and colons. Hyphenate complex modifiers: "zero-field-cooled magnetization." Avoid dangling participles, such as, "Using (1), the potential was calculated." [It is not clear who or what used (1).] Write instead, "The potential was calculated by using (1)," or "Using (1), we calculated the potential."

Use a zero before decimal points: "0.25," not ".25." Use "cm^3," not "cc." Indicate sample dimensions as "0.1 cm x 0.2 cm," not "0.1 x 0.2 cm^2." The abbreviation for "seconds" is "s," not "sec." Do not mix complete spellings and abbreviations of units: use "Wb/m^2" or "webers per square meter," not "webers/m^2." When expressing a range of values, write "7 to 9" or "7-9," not "7~9."

A parenthetical statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.) In American English, periods and commas are within quotation marks, like "this period." Other punctuation is "outside"! Avoid contractions; for example, write "do not" instead of "don't." The serial comma is preferred: "A, B, and C" instead of "A, B and C."

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The word "data" is plural, not singular. The subscript for the permeability of vacuum μ_0 is zero, not a lowercase letter "o." The term for residual magnetization is "remanence"; the adjective is "remanent"; do not write "remnance" or "remnant." Use the word "micrometer" instead of "micron." A graph within a graph is an "inset," not an "insert." The word "alternatively" is preferred to the word "alternately" (unless you really mean something that alternates). Use the word "whereas" instead of "while" (unless you are referring to simultaneous events). Do not use the word "essentially" to mean "approximately" or "effectively." Do not use the word "issue" as a euphemism for "problem." When compositions are not specified, separate chemical symbols by en-dashes; for example, "NiMn" indicates the intermetallic compound $Ni_{0.5}Mn_{0.5}$ whereas "Ni–Mn" indicates an alloy of some composition Ni_xMn_{1-x}.

Be aware of the different meanings of the homophones "affect" (usually a verb) and "effect" (usually a noun), "complement" and "compliment," "discreet" and "discrete," "principal" (e.g., "principal investigator") and "principle" (e.g., "principle of measurement"). Do not confuse "imply" and "infer."

Prefixes such as "non," "sub," "micro," "multi," and "ultra" are not independent words; they should be joined to the words they modify, usually without a hyphen. There is no period after the "et" in the Latin abbreviation "*et al.*" (it is also italicized). The abbreviation "i.e.," means "that is," and the abbreviation "e.g.," means "for example" (these abbreviations are not italicized).

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IX. Conclusion

A conclusion section is not required. Although a conclusion may review the main points of the paper, do not replicate the abstract as the conclusion. A conclusion might elaborate on the importance of the work or suggest applications and extensions.

Appendix

Appendixes, if needed, appear before the acknowledgment.

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References

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